Asian IBIS Summit

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On die De-cap Modeling Proposal

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Semiconductor & System Design Technical Committee
LPB Interoperable Design Sub-Committee

Modeling Working Group

Introduction

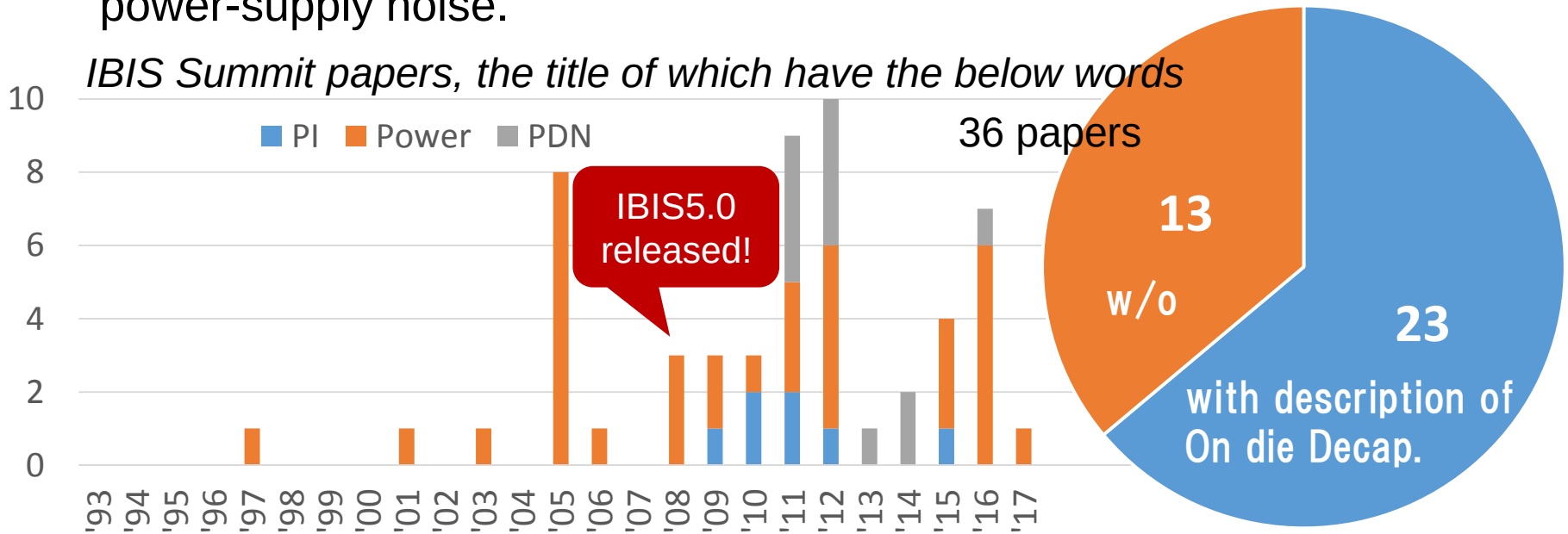
- Digital IF
  - Data rate enters the GHz range.
  - Supply voltage further declined.
    -> SI&PI&EMI Analysis became much more important.

- Added Keywords in IBIS Version 5.0
  - [Composite Current]:Consumption current IT-Waveform.
  - [ISSO PU(PD)]:Characteristic between supply voltage and PU.
    -> IBIS is now useful for Chip PDN-aware SI&PI&EMI analysis.

Chip PDN characteristic

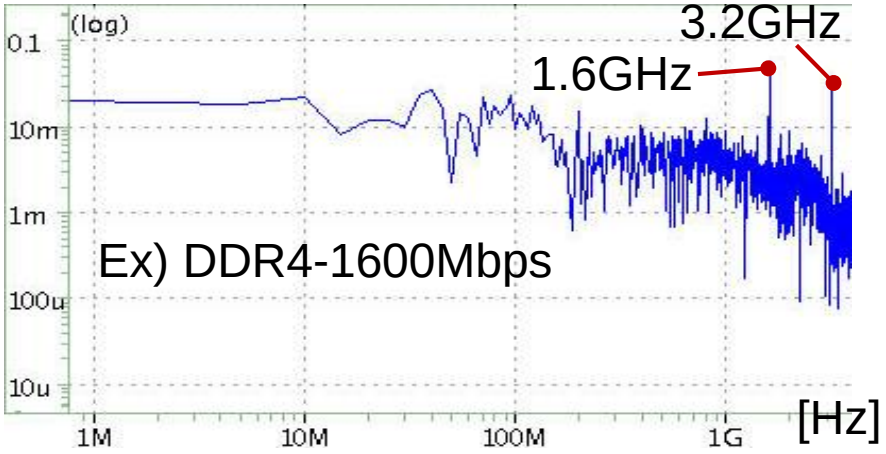
- However, Almost all IBIS models don't have Chip PDN characteristic.
  - On die Resistance affects IR-Drop and Q factor.
  - On die De-cap affects High frequency power-supply noise.

Many papers reported in IBIS Summit describe importance of On die De-cap, because it is one of the few solution that reduce high frequency power-supply noise.

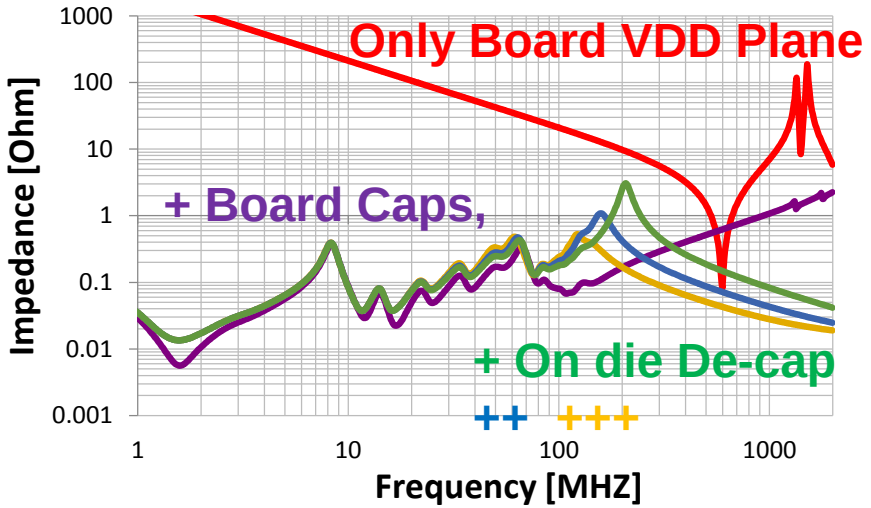


On die De-cap impact

- The frequency spectrum of high speed digital IF consumption current depends on its data rate.



- To reduce impedance of high frequency range makes supply-voltage quality better.



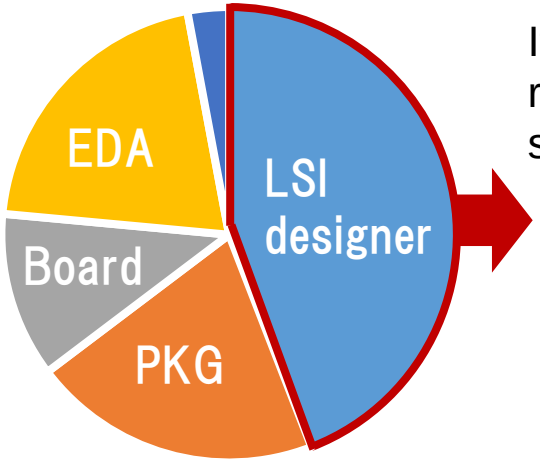
-> Only On die De-cap can affect supply voltage quality in high frequency range.

A Survey of On die De-cap model

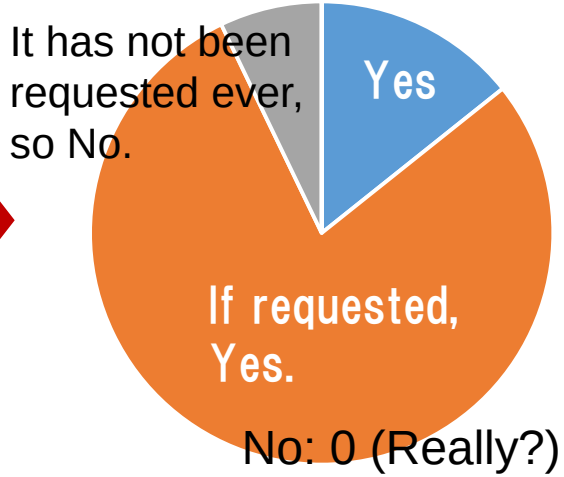
- But, board and system designers can hardly obtain On die De-cap model.

A Survey by JEITA LPB-SC MDL-WG @LPB developpers workshop 2017.9.2

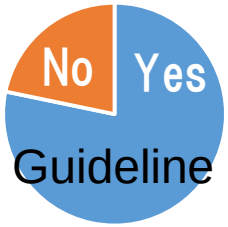
Respondents

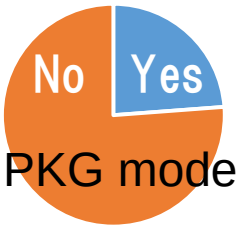


to LSI designer "Did you offer On die De-cap model?"



to All "Can you obtain information about Chip PDN?"



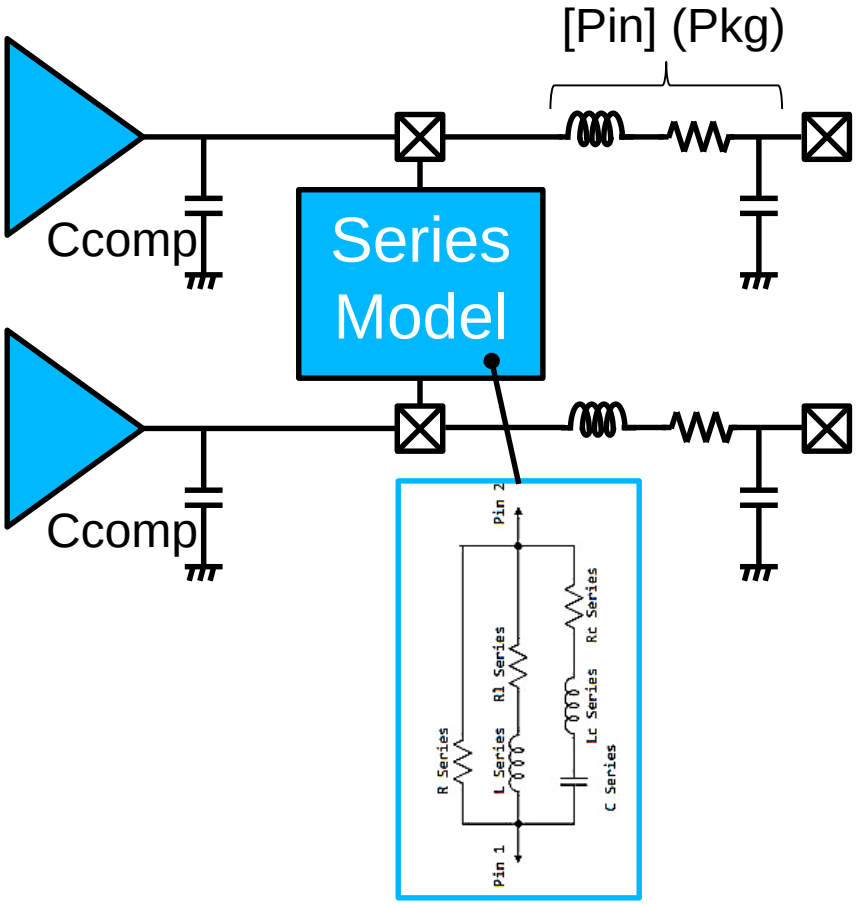


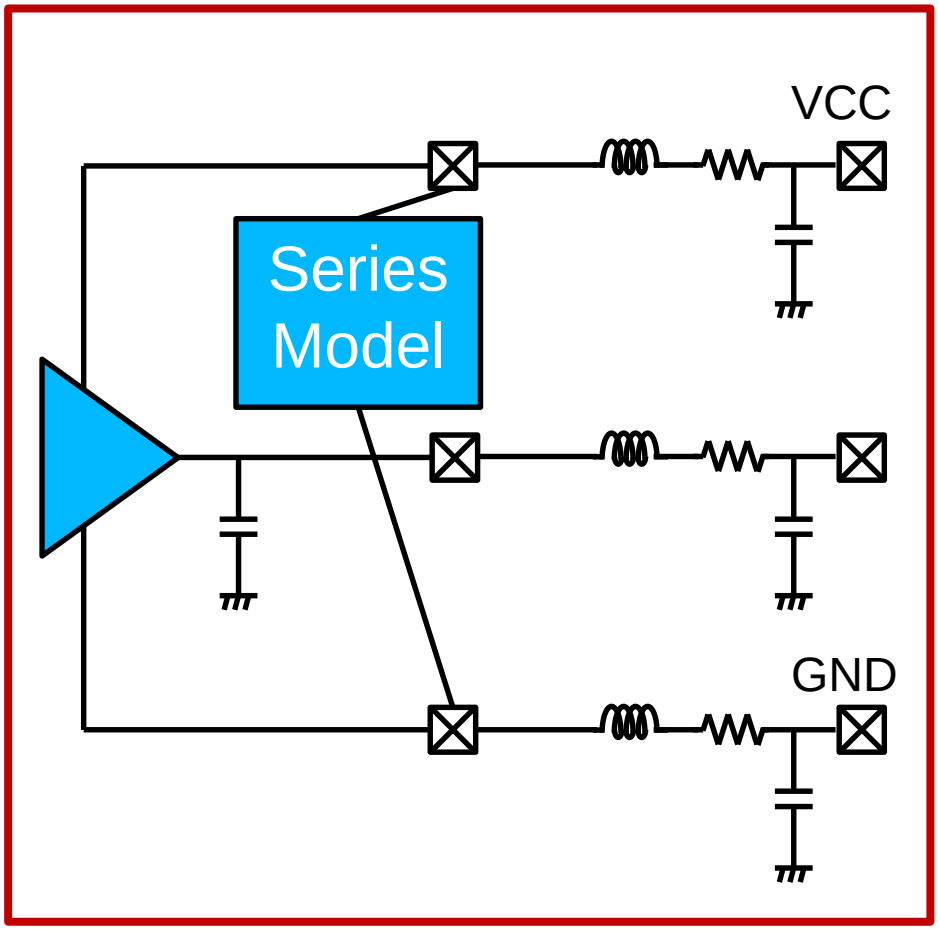
- In some cases LSI designers offer On die De-cap model on request.
  And they wonder "Which model format is suitable for our customer?"
  -> It's time to add new IBIS keywords about On die De-cap!

On die De-cap model in IBIS

'Modeling the On-die De-cap of IBIS5.0 PDN-aware Buffers'
Lance Wang, and Randy Wolff Nov 2011

[Model]
Model_Type Series





On die De-cap model format proposal

```
[Pin]
A1  VCC  POWER
A2  VCC  POWER
B2  SigA  BufferA
C3  VSS  GND
C4  VCC  POWER
|
[Pin Mapping]
A1  NC       VBUS1
A2  NC       VBUS1
B2  GBUS1  VBUS1
C3  GBUS1  NC
C4  NC       VBUS2
|
[Series Pin Mapping]
C3  A1  OnChipDecap
|
[Model]  OnChipDecap
Model_type  Series
[C series]   3n  2.9n  3.1n
…
```

The word "Series" doesn't make me imagine PDN model.

```
[Pin]
A1  VCC  POWER
A2  VCC  POWER
B2  SigA  BufferA
C3  VSS  GND
C4  VCC  POWER
|
[Pin Mapping]
A1  NC       VBUS1
A2  NC       VBUS1
B2  GBUS1  VBUS1
C3  GBUS1  NC
C4  NC       VBUS2
|
[PDN Model Mapping]
C3  A1  OnChipDecap
|
[Model]  OnChipDecap
Model_type  PDN
[C]   3n  2.9n  3.1n
…
```

Proposal.
Only for PDN model.
Function is the same.

Another method

- [External Model] or [External Circuit] can reference other files which are written using the SPICE or IBIS-ISS.

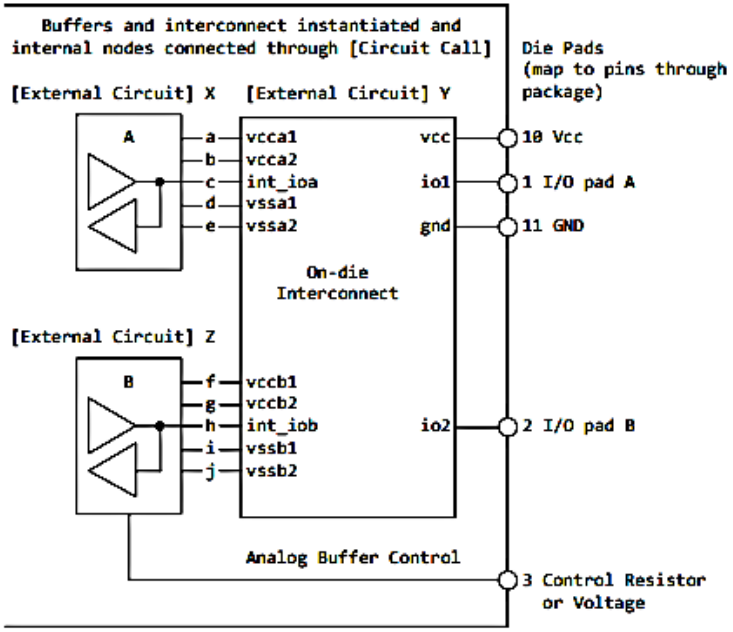
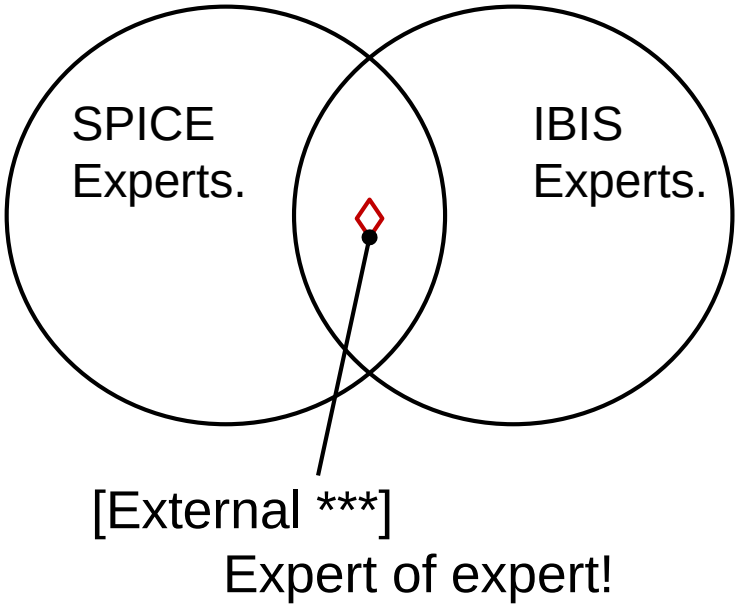


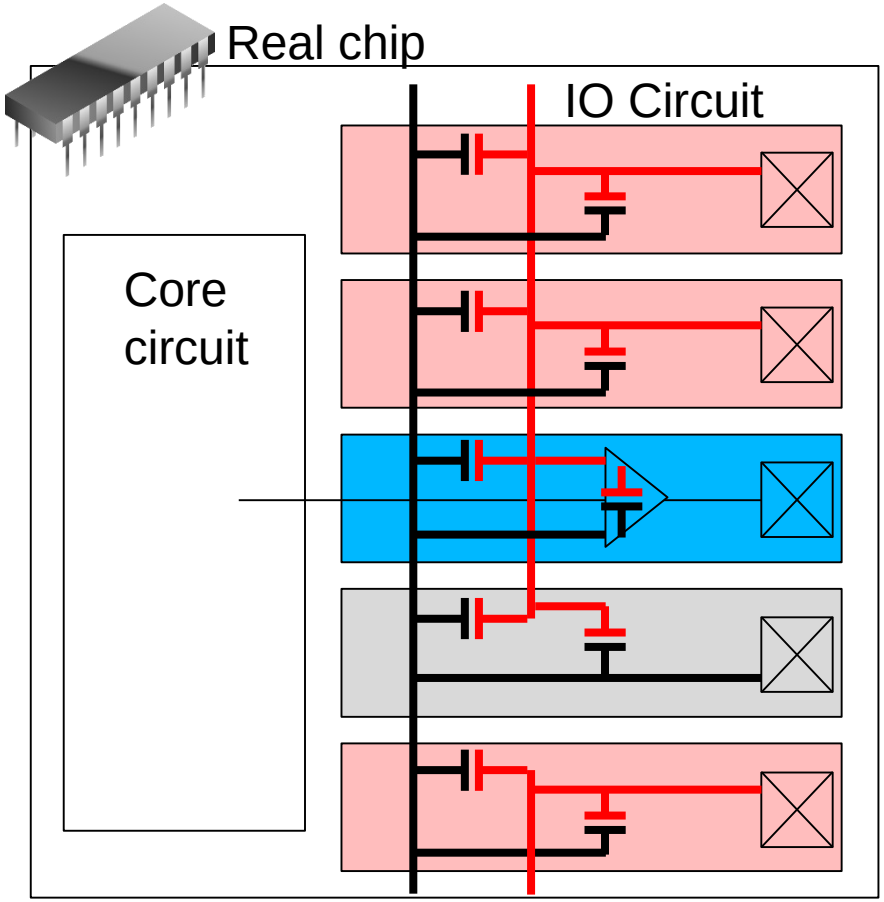
Figure 21 - Example Showing [External Circuit] Ports

too complex.

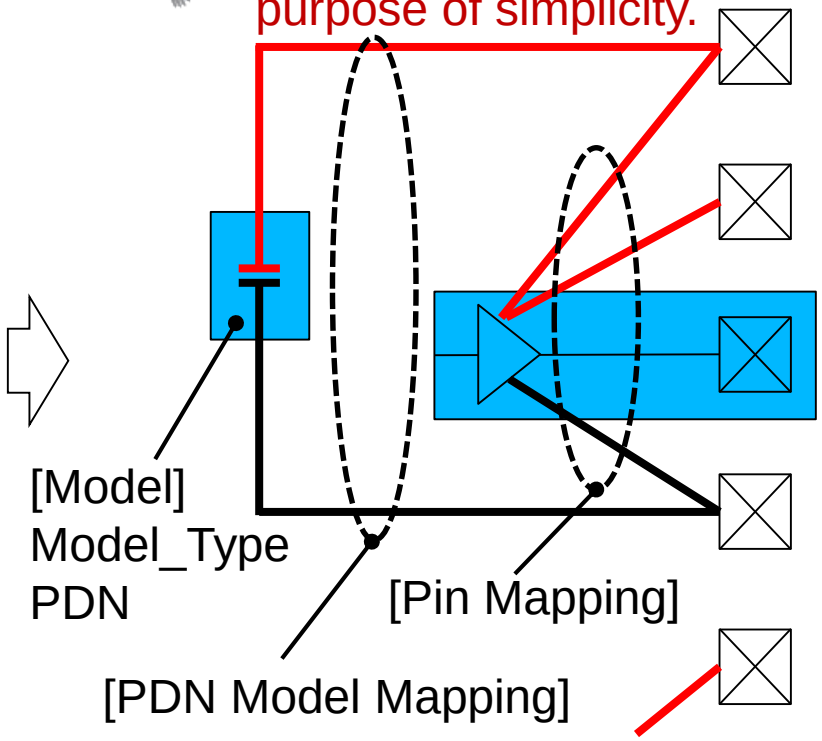


On die De-cap model and real circuit

- There are De-cap cell, parasitic capacitance between VCC metal and GND metal, and MOS capacitance in IO circuit of real chip.



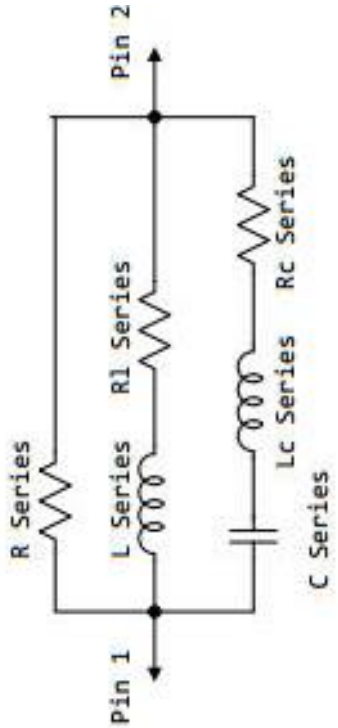
It is better to be represented by only one capacitor for the purpose of simplicity.



Topology of On die De-cap model

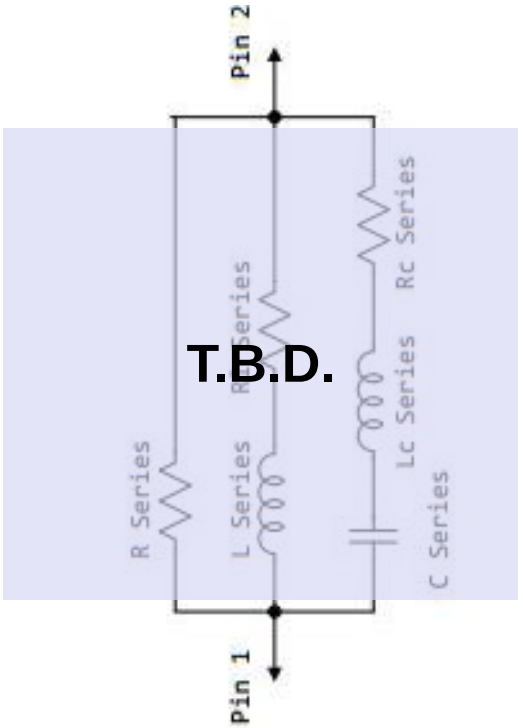
- Model_Type Series

IBIS maker can choose which element to enable. There are 30 circuit topologies.



- Proposal: Model_Type PDN

Only one topology available. (T.B.D.)



Modeling On die De-cap

- I hope that chip vendor can easily provide On die De-cap model by this proposal.
- However, even if this proposal is adopted, it takes some time to spread this model.

"I want to know this chip's PDN model right now!"
-> Try measuring.

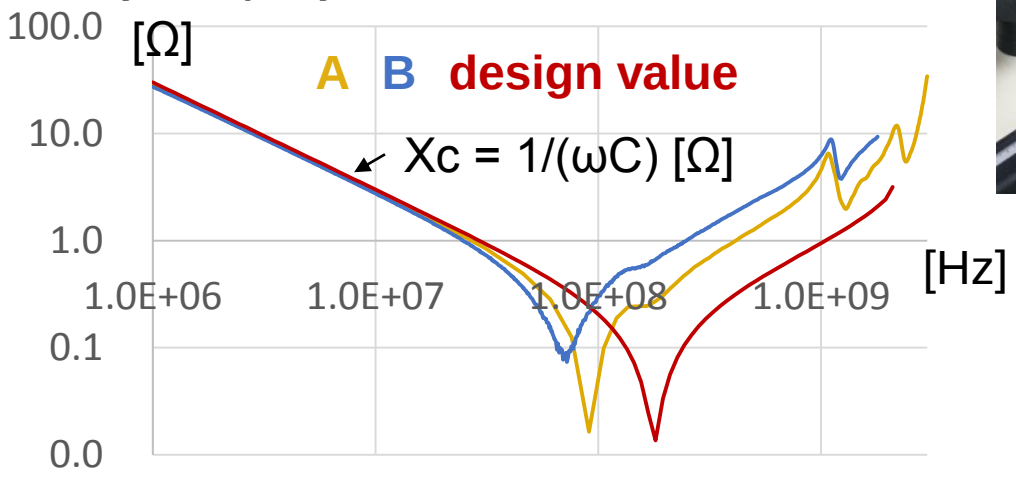
Measuring On die De-cap model

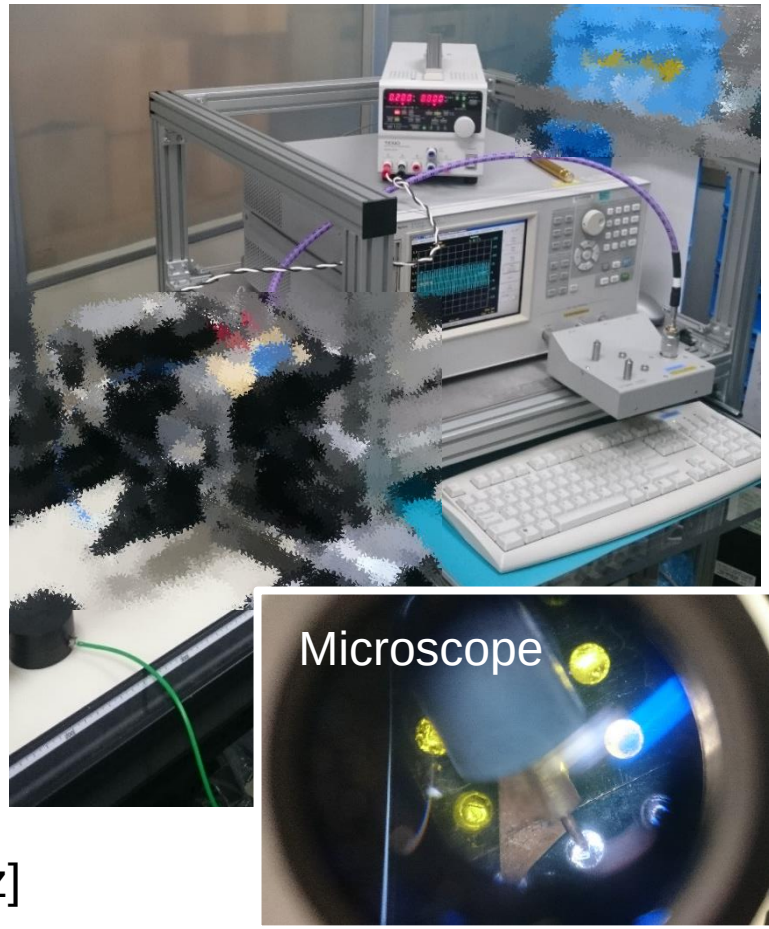
- Method

We measured impedance between VCC pin and GND pin by Impedance analyzer (or Network analyzer) .
Supply voltage was applied these pins also.

- Result

Measurement result of company A's ASIC by companyA and B





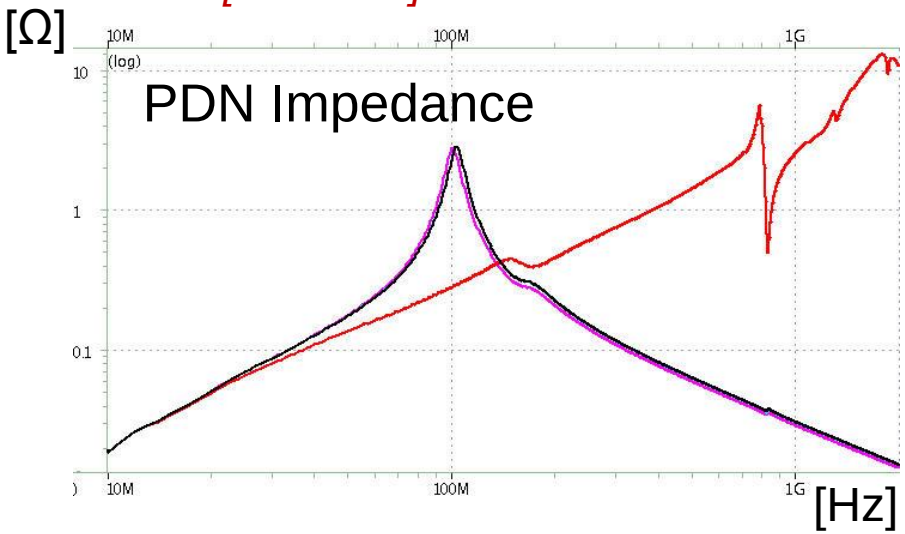
Correlation

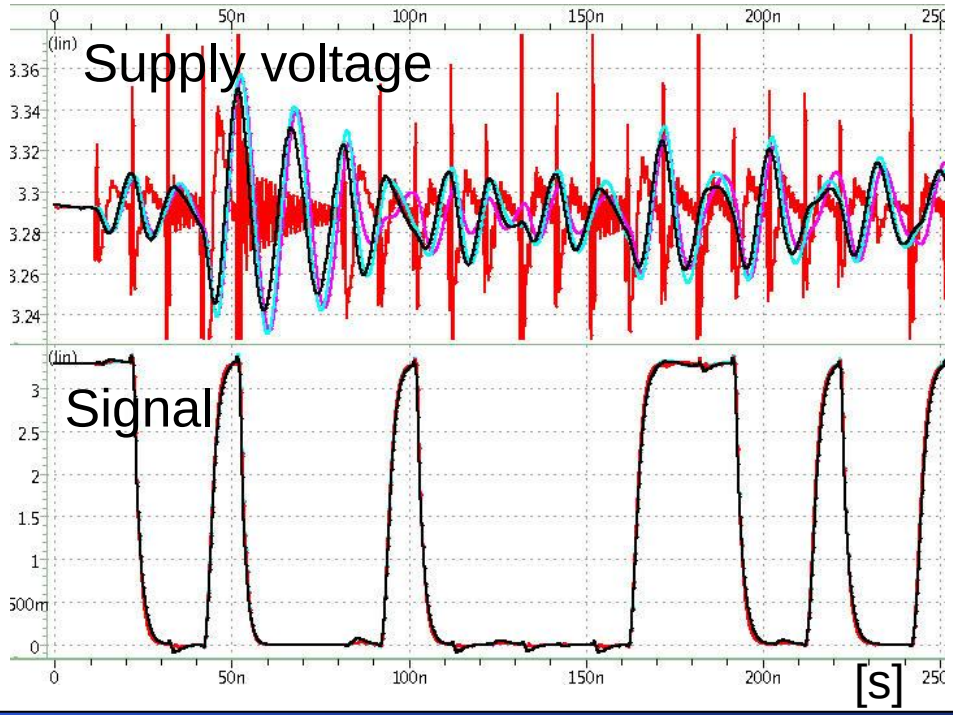
- Provisional On die De-cap model : One capacitor. ⏚

[Series Pin Mapping]
C3 A1 OnChipDecap
[Model] OnChipDecap
Model_type Series
[C series] XXX

①Measurement：5.55nF
②Design value：5.25nF
③Without De-cap:0nF

④SPICE IO model +
Design value：5.25nF





JEITA LPB-SC MDL-WG

- LPB Sub-Committee Modeling working group

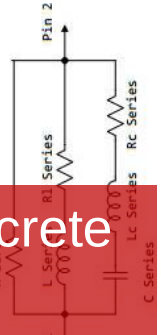
  We have been studying SI, PI, EMI, and Thermal simulation model problems for proposing new models to solve them and promoting standardization.

- Contents of activities in 2017
  - Survey of On die De-cap model availability
  - Standardization of On die De-cap measuring method
  - Proposal of measured On die De-cap model's circuit topology
  - Proposal of IBIS On die De-cap model

10th LPB Forum

- “LPB”
  - stands for LSI & Package & Board. When new products are produced or for creating competitive products, plan, design, production for LPB went closely coordinated to each other, and we are working hard to aim for win-win.

- “LPB Forum”
  - Introduces case examples of Interoperable design
  - 9th LPB Forum’s papers.
    LPB format overview
    A case example of conceptual design with LPB format
    IBIS-LPB design kit
    PI analysis with LPB format and IBIS5.0
  - 10th LPB Forum date：2018.3.9 Fri.



Proposal of concrete circuit and Measurement & Sim. Additional case introduction planned.

Conclusion

It has long been known that the chip's characteristics have a large influence on the whole PDN.

However, chip PDN model still is not widespread. Therefore, We proposed to add explicit keywords of chip PDN to IBIS.

We confirmed that these keywords improve SI “Power Aware” simulation. And we introduced On die De-cap measuring method.

After we will study modeling from measurement, We will propose concrete circuit.

Thank you!