# A potential application of IBIS to CISPR25 based EMI analysis of DCDC converter

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- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary



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## Motivation and objective

- EMI simulation of IBIS modeled DCDC converter
- ✓ Study on modeling to comply with CISPR25
- ✓ Initial trial with bare IBIS descriptions
- → Simulation results show discrepancies from measurements
- Make discussions on source of errors and solutions

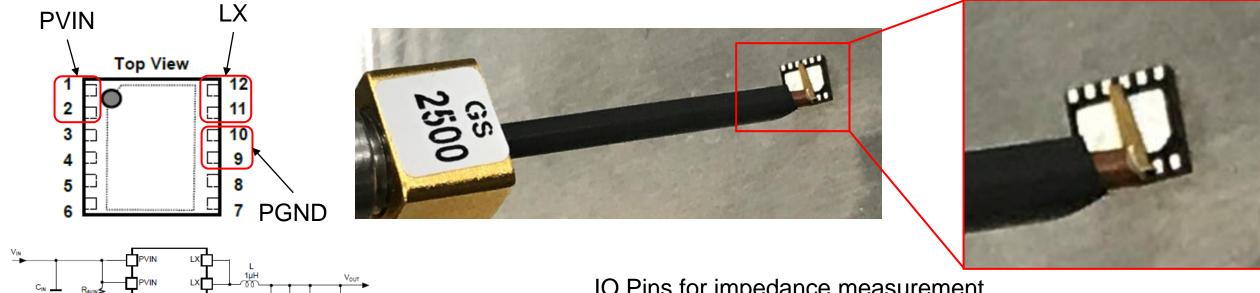


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#### DCDC converter impedance measurement

DCDC converter: RICOH RP510L004N-TR-A



IO Pins for	· impedance	measurement
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Pin(S-G)	No.(S-G)	Pitch(mm)	Bias voltage(V)	Freq.(Hz)※
PVIN-PGND	PIN2-PIN10	2.65mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
PVIN-LX	PIN2-PIN11	2.6mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
LX-PGND	PIN11-PIN10	0.5mm±0.1mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G

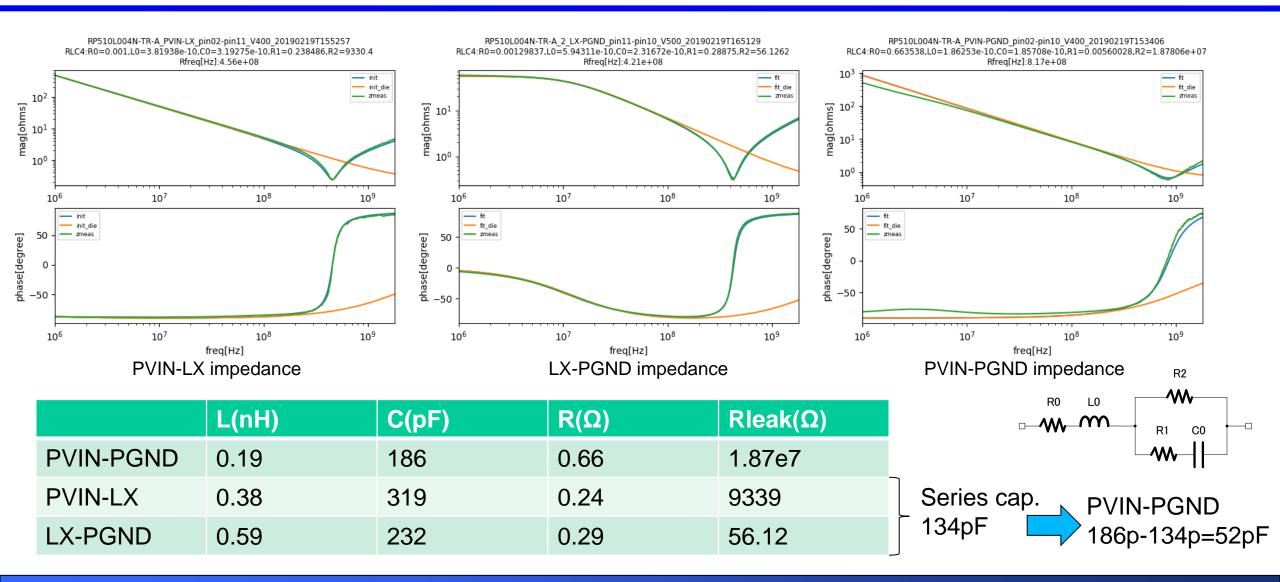
%Frequency depends on equipments

cf.) https://www.e-devices.ricoh.co.jp/en/products/power/dcdc/rp510/rp510-ea.pdf



**Typical Application Circuit** 

## Impedance measurement and equivalent circuit





## Capacitance description in IBIS format

Specify the measured caps as C\_comp\_pullup, C\_comp\_pulldown in the IBIS format.

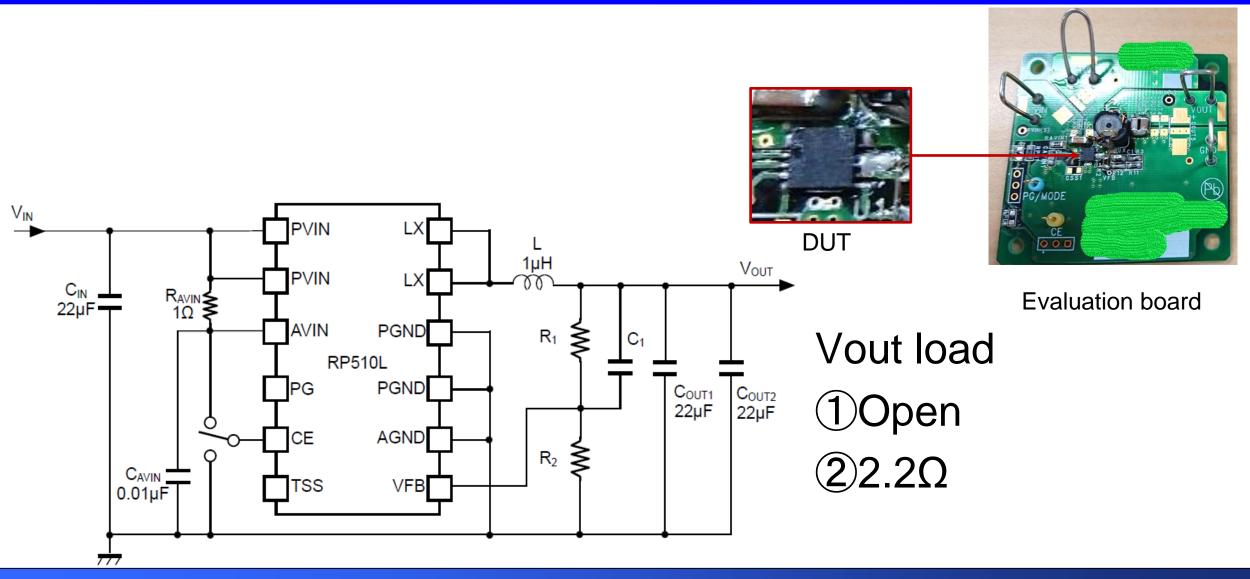
In case that large discrepancy appear in the total capacitance, need to regenerate IBIS model adding supplemental capacitance to the spice netlist.



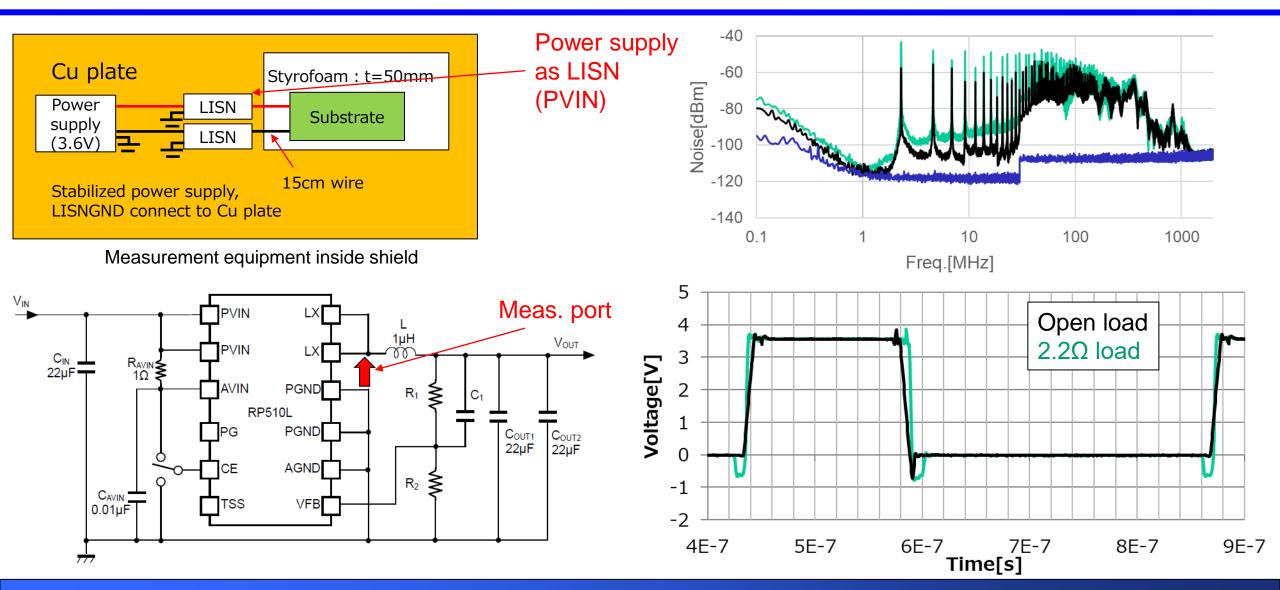
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#### Measurement circuit construction



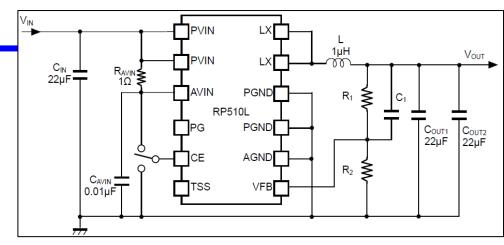
#### Measurement environment and results

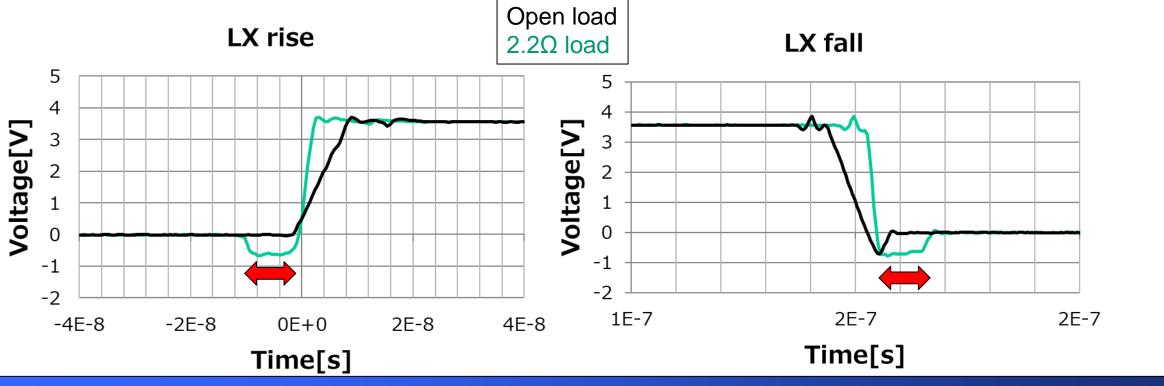




#### Measured LX waveform

Dead time appears in LX waveform with resistive load





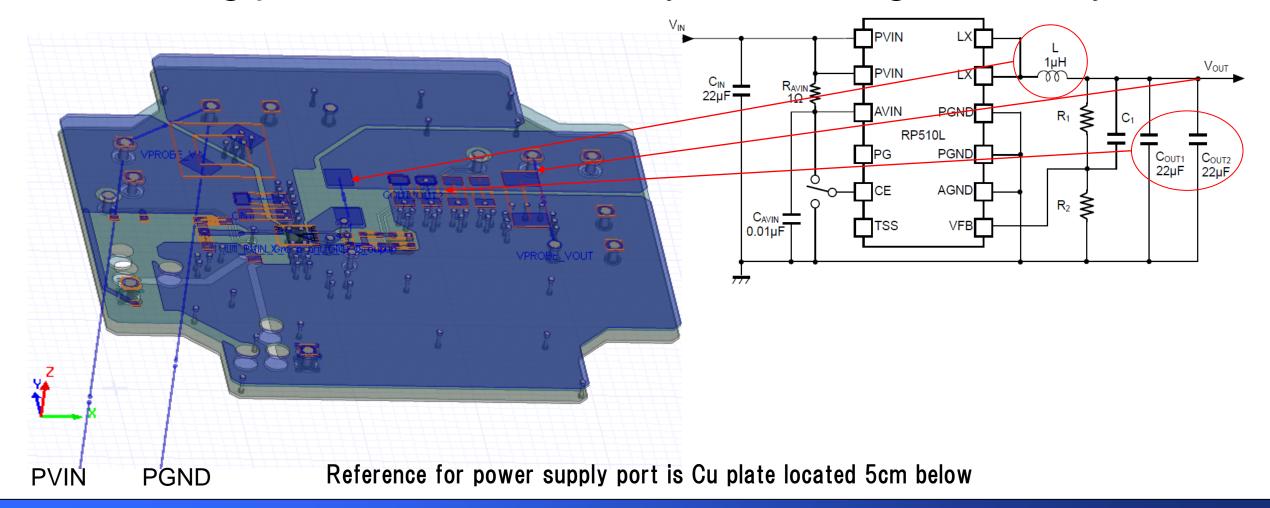


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#### Printed circuit board model

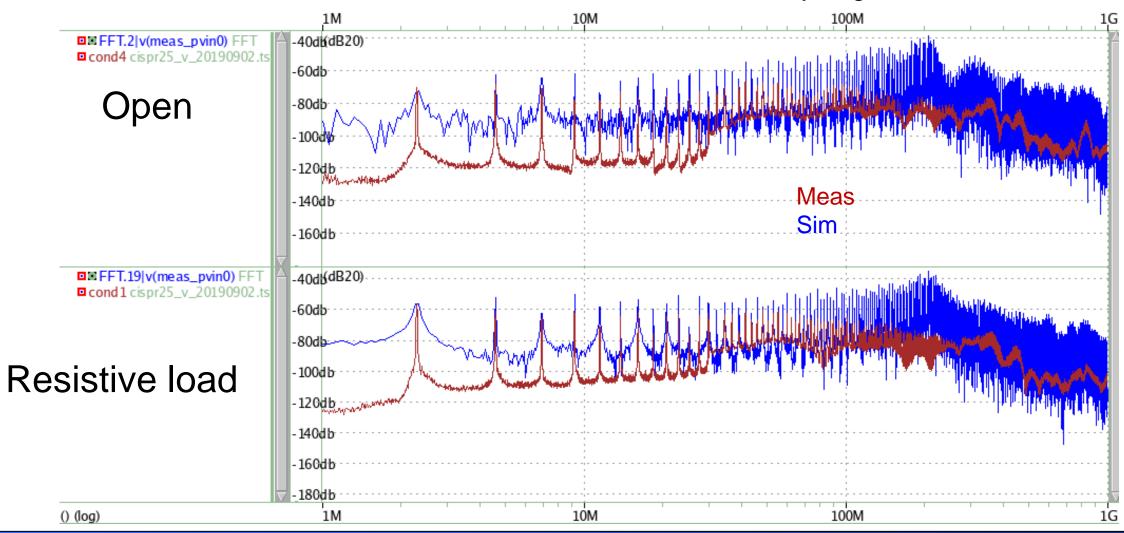
#### Modeling printed circuit board by electromagnetic analysis





#### Simulation results vs Measurement

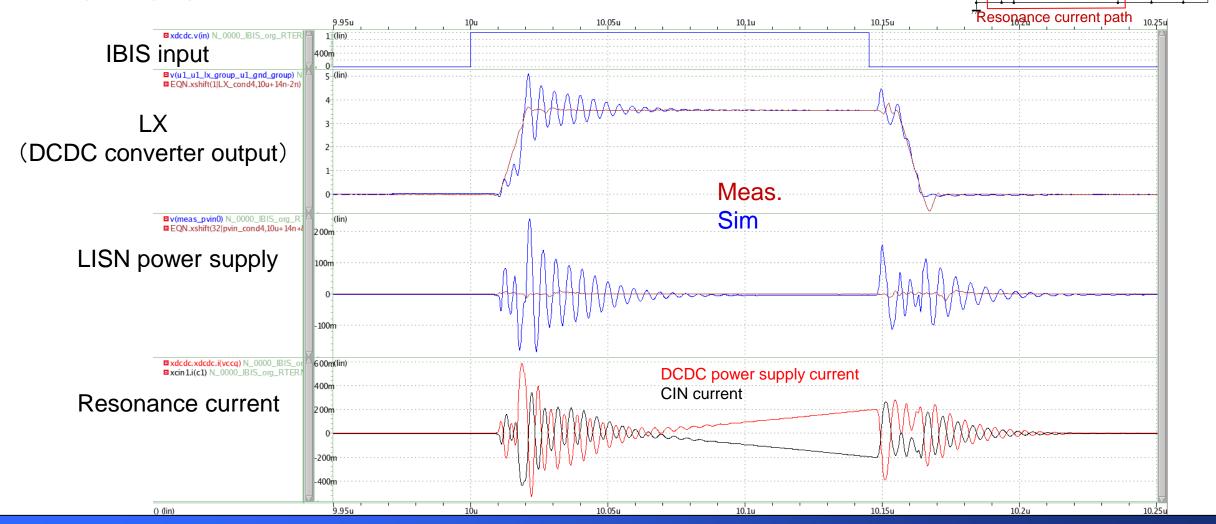
The difference between simulation and actual measurement is very large





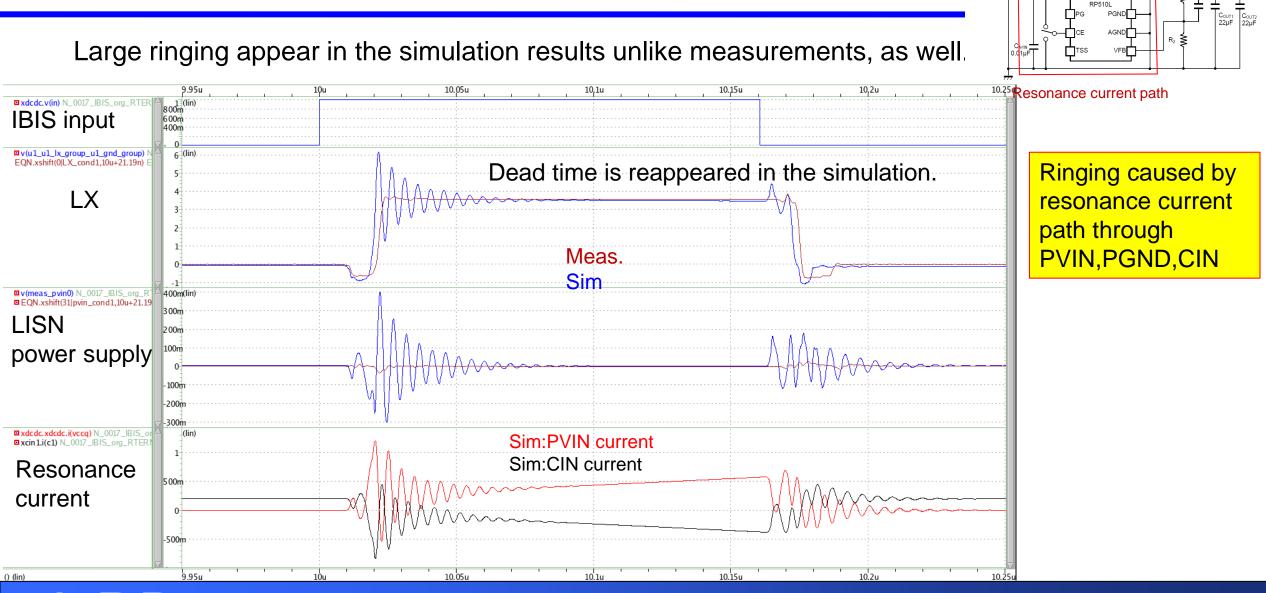
# Simulation results: Open

Large ringing appear in the simulation results unlike measurements.



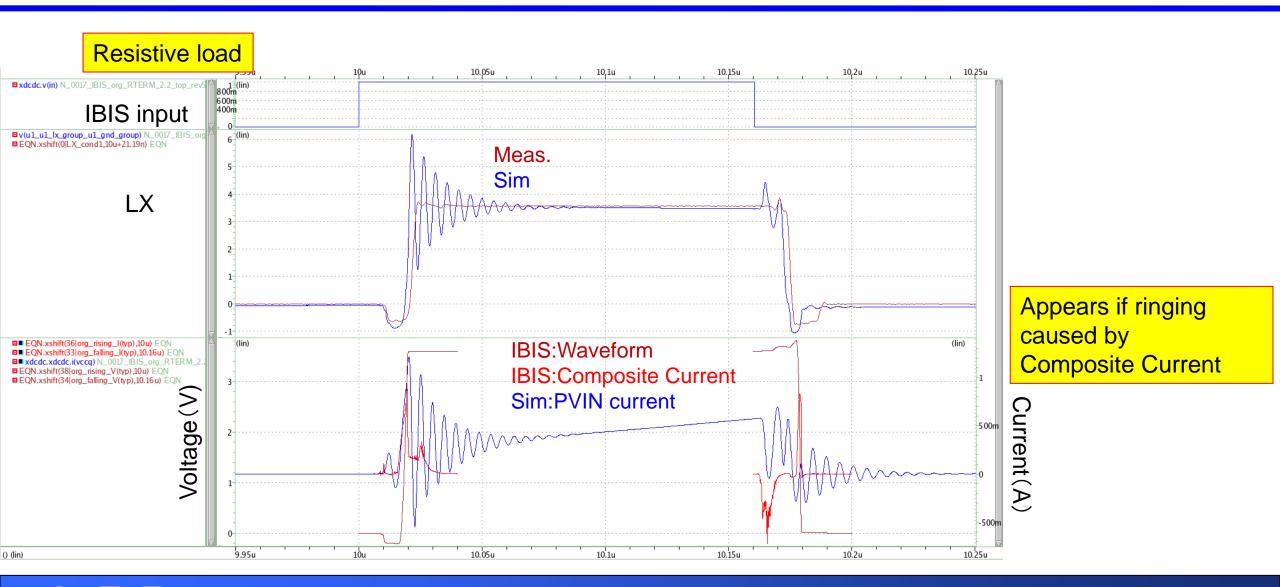


#### Simulation results: Resistive load





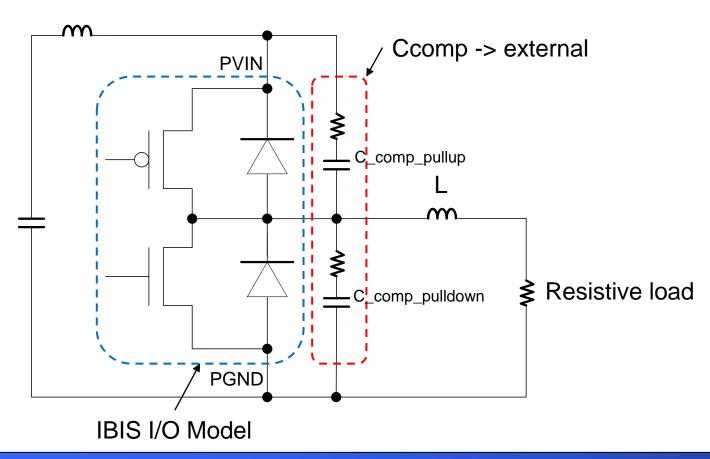
#### Dependence on Rising/Falling Waveform, composite current defined in IBIS

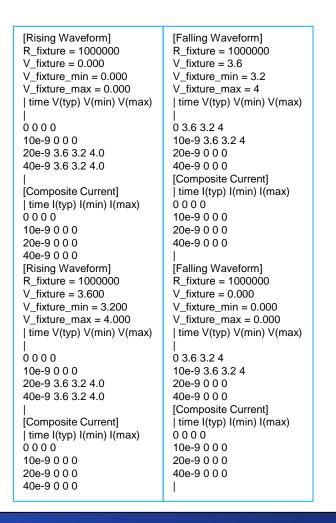




#### Changing Rising/Falling Waveform, Composite current

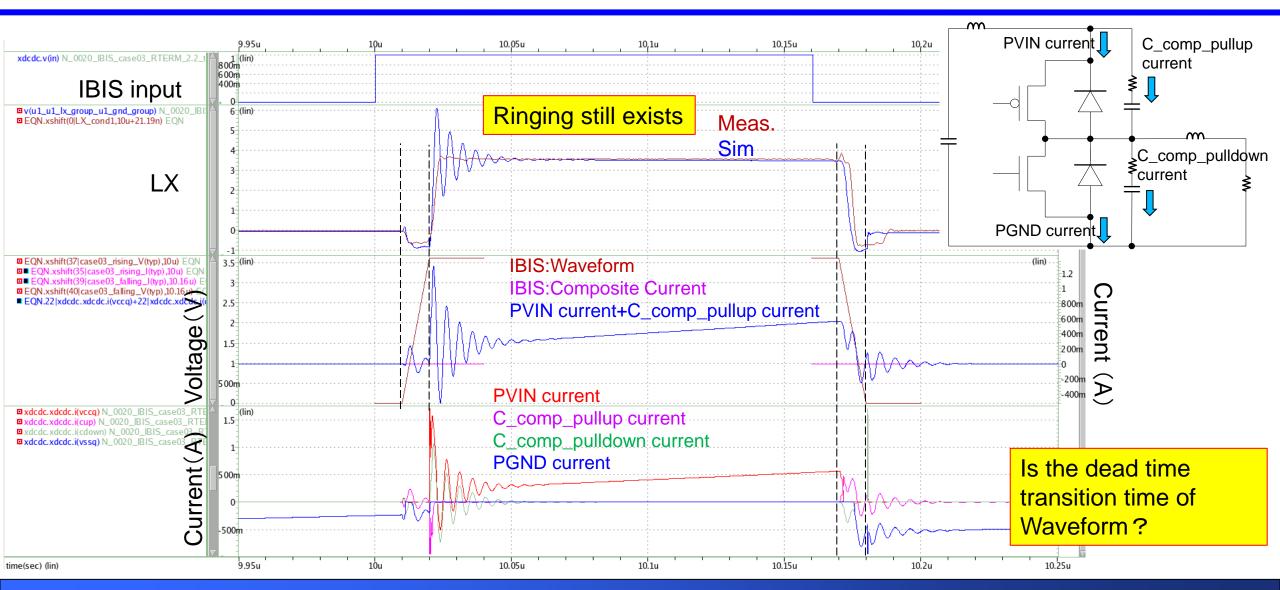
Make Ccomp external, Composite Current 0A, and Waveform simple rise/fall, respectively





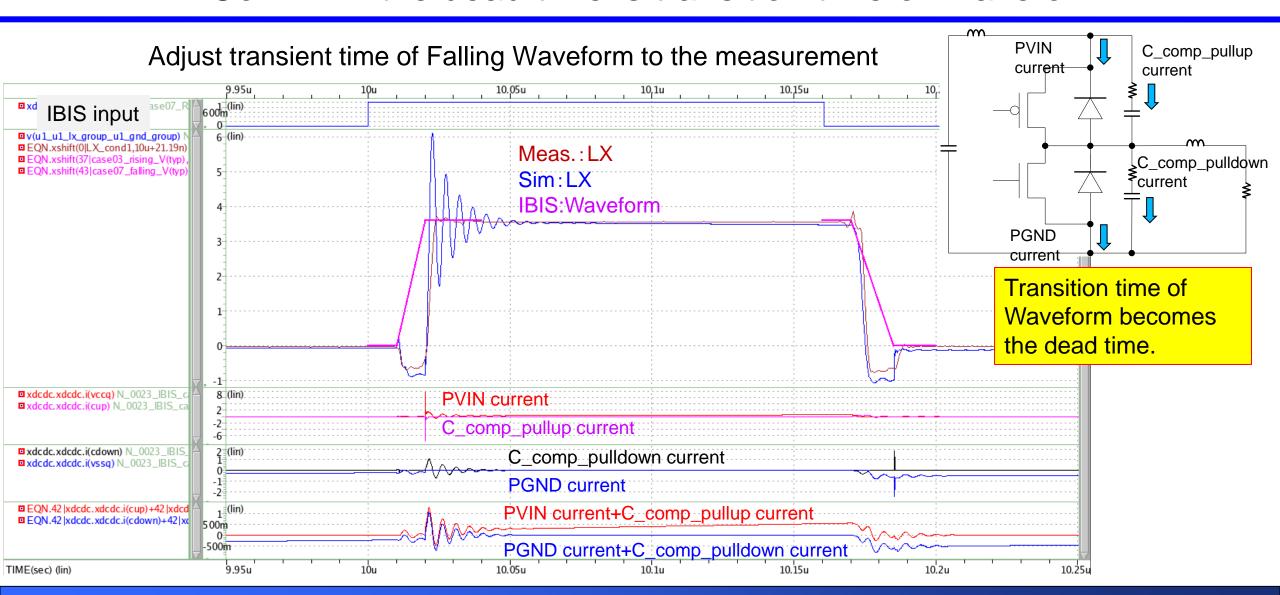


#### Resistive load: Dependence on Rising/Falling Waveform, Composite current





#### Confirm if the dead time is transition time of Waveform

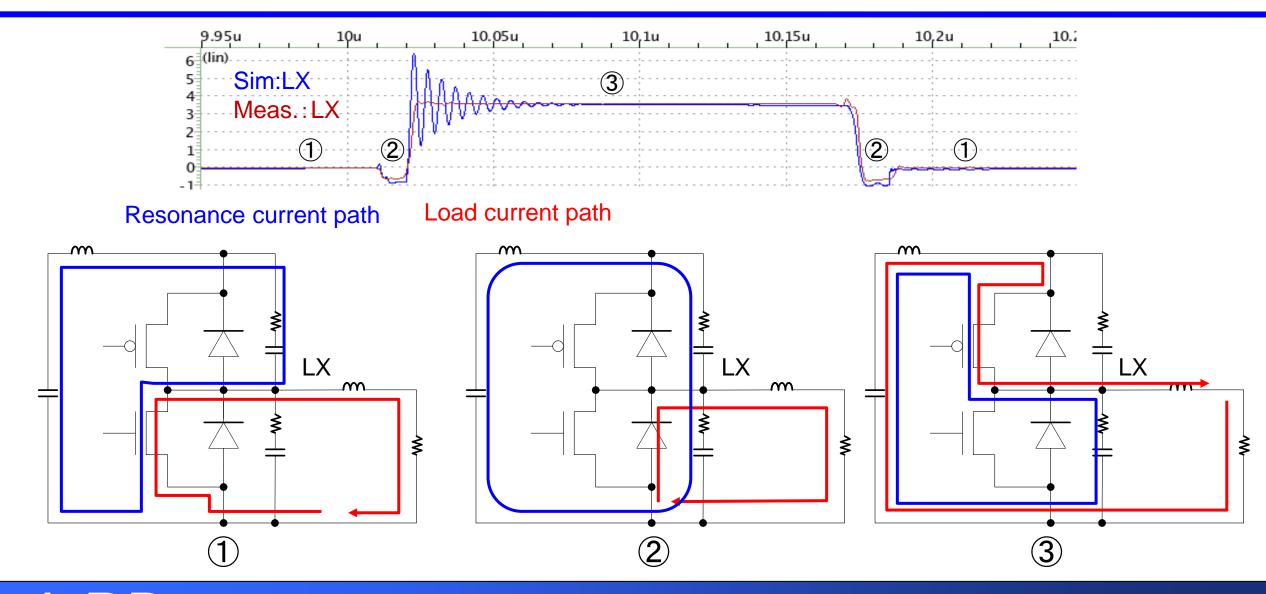




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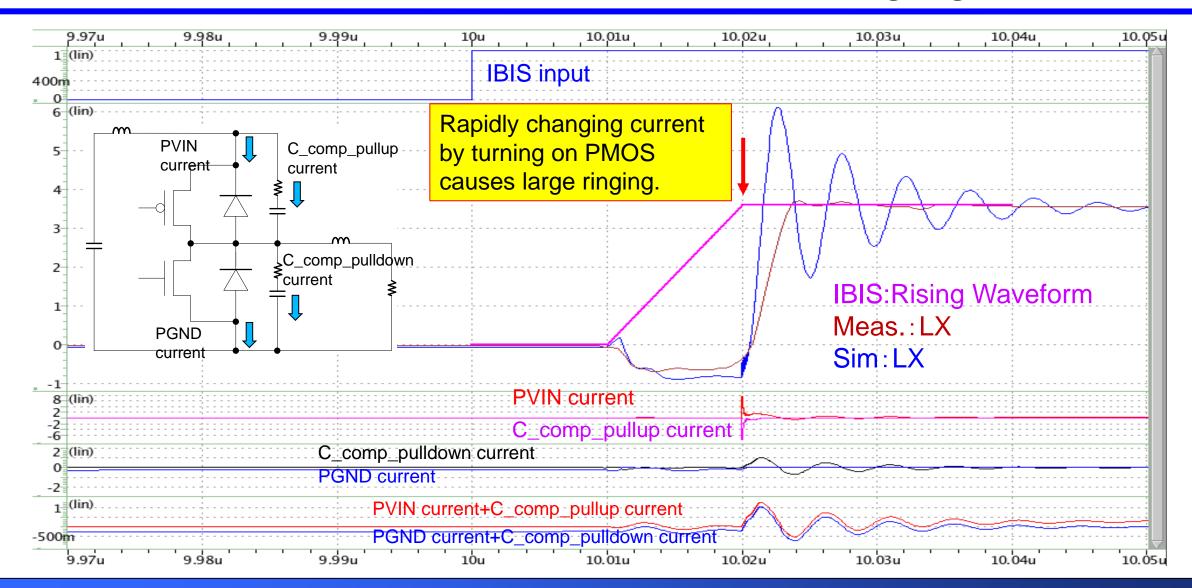


#### Discussion: Load current path and resonance current path





# Discussion: Cause of the ringing





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## Summary

- Trial to simulate CISPR25 for IBIS described DCDC
- Discrepancies from measurements in high frequency range
- ✓ Possible source of error in the simulation: Large ringing induced by instantly switching MOS transistors
- Mitigating unrealistic transitions is considered to be a dominant solution.



#### Possible improvements

 Retrieve Waveform and Composite Current in IBIS by SPICE simulation adjusted the load conditions

cf.) https://ibis.org/summits/nov08a/chen.pdf

```
2EQ/2UK \ algorithm \ Vwaveform(t) \ Vdie(t) \ Vdie(t) \ L_{fixture} \ R_{fixture} \ V_{fixture} \ R_{fixture} \
```

Obtain Rising/Falling Waveform and Composite Current directly from measurement

