A further study on the application of IBIS to CISPR25 based EMI analysis of DCDC converter ～Resolving unexpected ringing in the waveform～

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Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Study on the discrepancy from the measurement
  - From IBIS model to Spice macro model
  - Improving the Spice macro model
- Summary
- Remaining issues and plans

Motivation and objective

Most power device models are provided as Spice models dedicated to specific circuit simulators

→ Can not freely choose a circuit simulator

Potential limitation by expression of each circuit simulator

If the power device model can be represented with IBIS

→ Can freely choose a circuit simulator

Can improve usability by gaining regularity

Furthermore, if the IBIS model can be derived from measurement

→ Modeling made easier

JEITA IBIS-TG studies IBIS modeling of a power device DCDC converter, targeting to EMI simulation (CISPR25 conducted noise simulation)

In this presentation, we discuss error caused in the IBIS based DCDC noise simulation compared to the measurement, reported at 2019 Asian IBIS Summit (TOKYO, JAPAN)

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DCDC converter impedance measurement

DCDC converter: RICOH RP510L004N-TR-A

PVIN

LX

PGND

Top View

Typical Application Circuit
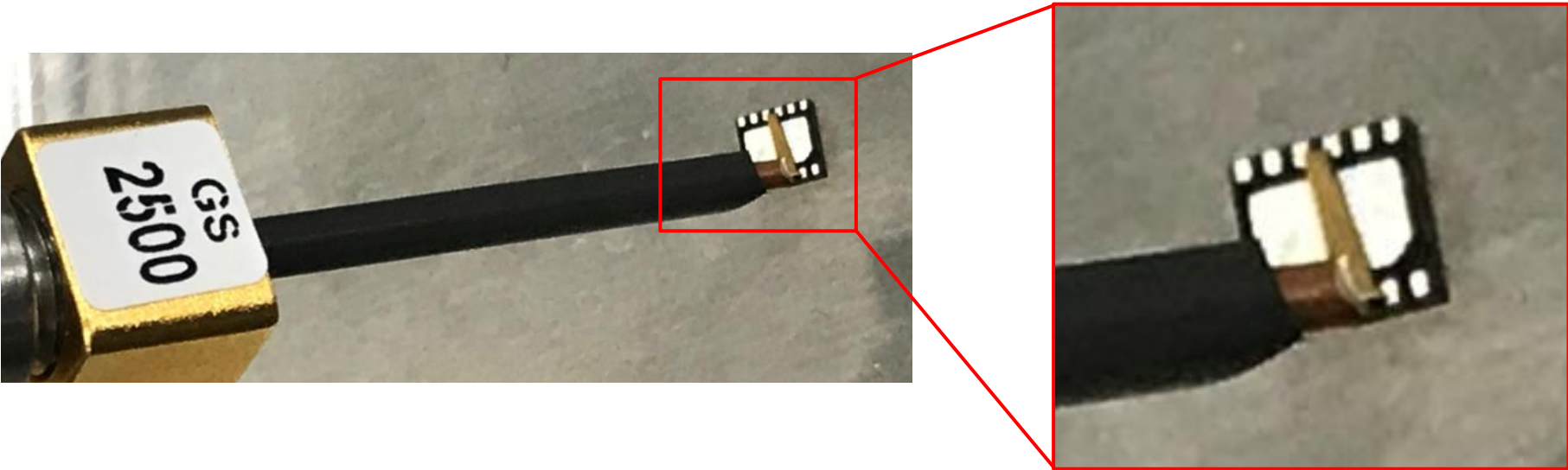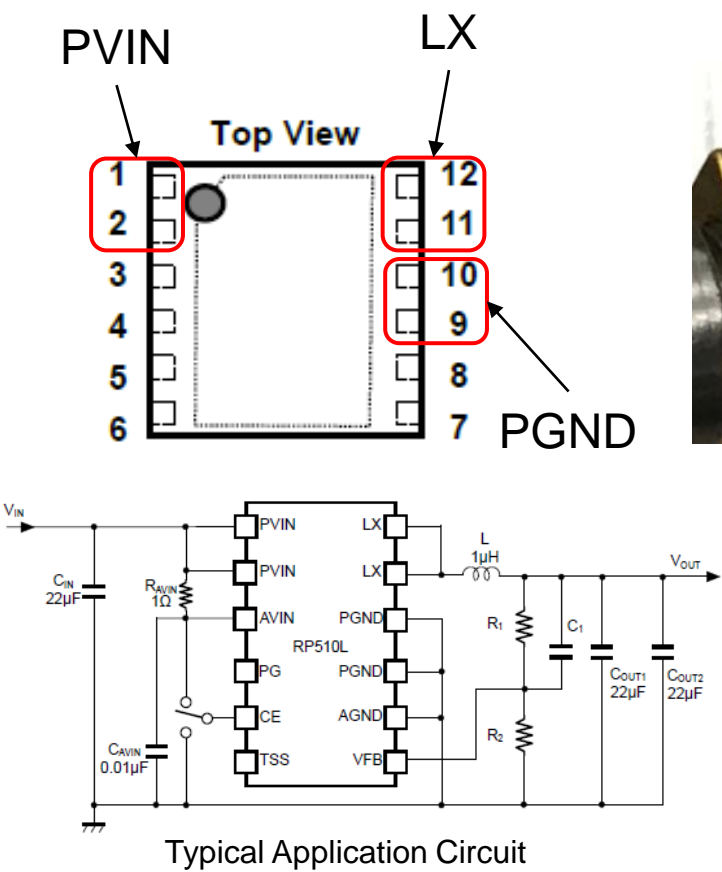
IO Pins for impedance measurement

Pin（S-G）	No.（S-G）	Pitch(mm)	Bias voltage（V）	Freq.（Hz）※
PVIN-PGND	PIN2-PIN10	2.65mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
PVIN-LX	PIN2-PIN11	2.6mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
LX-PGND	PIN11-PIN10	0.5mm±0.1mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G

※Frequency depends on equipment
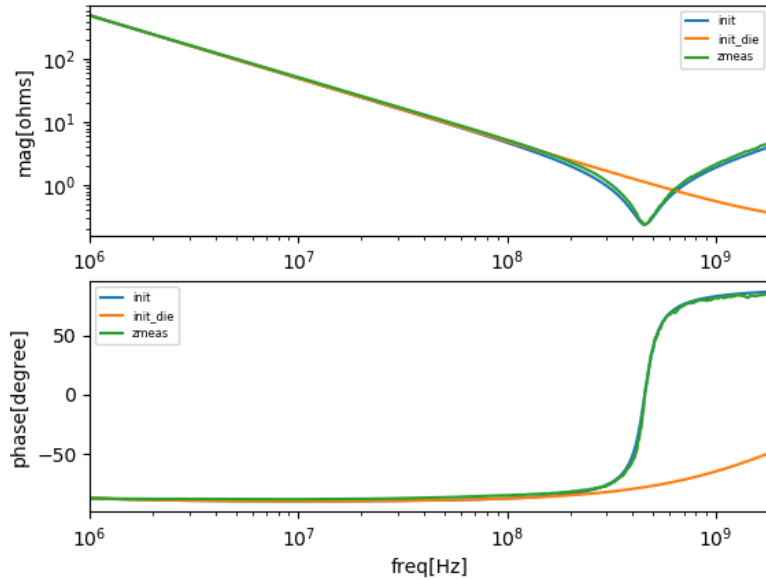
cf.) https://www.e-devices.ricoh.co.jp/en/products/power/dcdc/rp510/rp510-ea.pdf

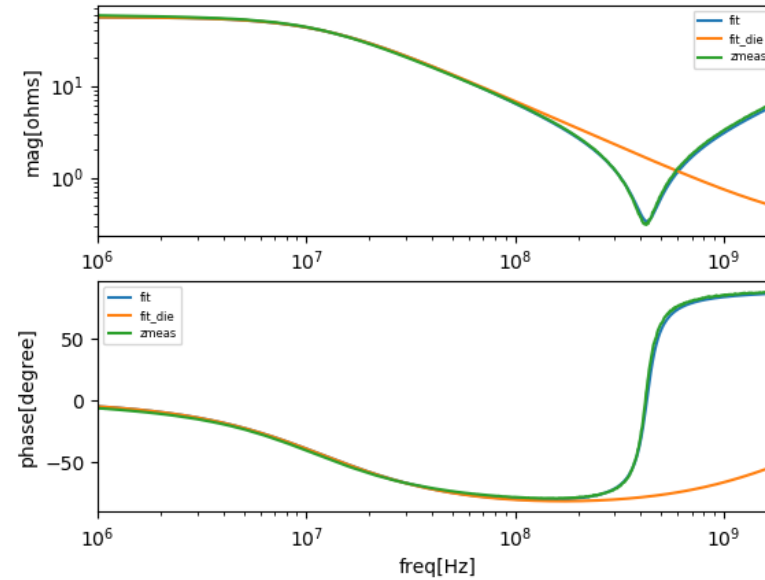Equipment used in this report: HP4291A

Impedance measurement and equivalent circuit

RP510L004N-TR-A_PVIN-LX_pin02-pin11_V400_20190219T155257
RLC4:R0=0.001,L0=3.81938e-10,C0=3.19275e-10,R1=0.238486,R2=9330.4
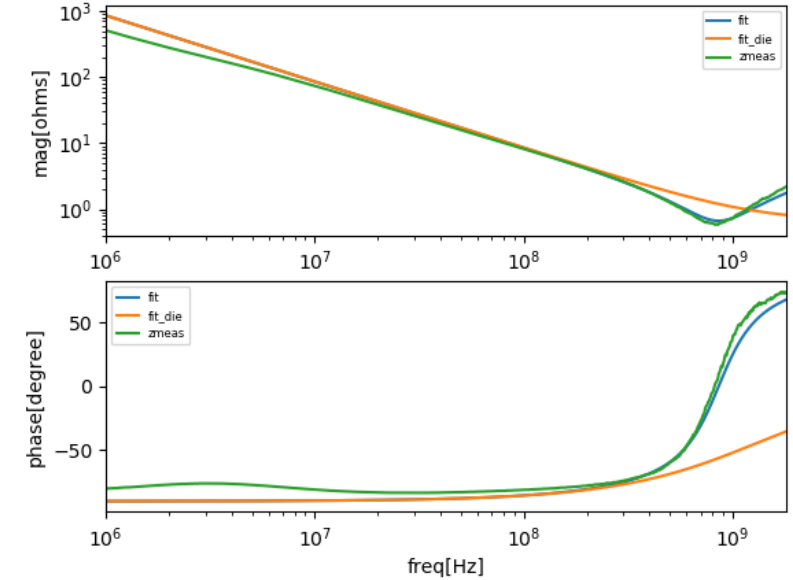Rfreq[Hz]:4.56e+08

RP510L004N-TR-A_2_LX-PGND_pin11-pin10_V500_20190219T165129
RLC4:R0=0.00129837,L0=5.94311e-10,C0=2.31672e-10,R1=0.28875,R2=56.1262
Rfreq[Hz]:4.21e+08

RP510L004N-TR-A_PVIN-PGND_pin02-pin10_V400_20190219T153406
RLC4:R0=0.663538,L0=1.86253e-10,C0=1.85708e-10,R1=0.00560028,R2=1.87806e+07
Rfreq[Hz]:8.17e+08

PVIN-LX impedance
(HighSide)

LX-PGND impedance
(LowSide)

PVIN-PGND impedance

	L(nH)	C(pF)	R(Ω)	Rleak(Ω)
PVIN-PGND	0.19	186	0.66	1.87e7
PVIN-LX	0.38	319	0.24	9339
LX-PGND	0.59	232	0.29	56.12
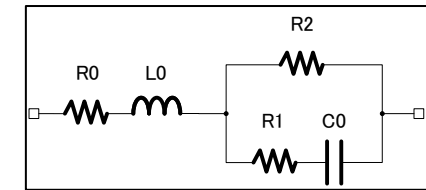
Series cap.
134pF

PVIN-PGND
186p-134p=52pF

Capacitance description in IBIS format

Specify the measured caps as C_comp_pullup, C_comp_pulldown in the IBIS format.
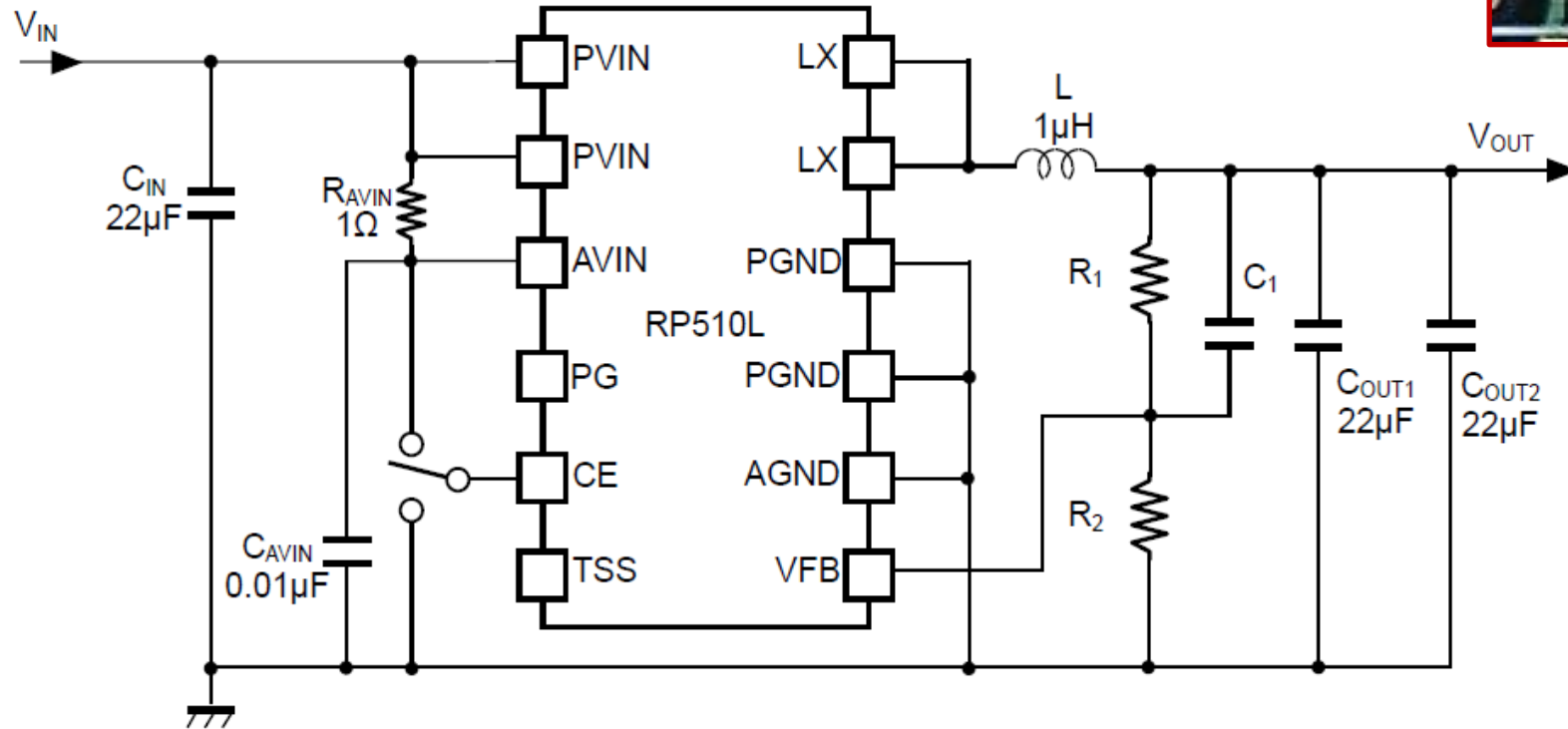
```
[Model]    bbb
Model_type      I/O
Polarity        Non-Inverting
Vinl         = .72000000
Vinh         = 2.88000000
Vmeas        = 1.80000000
|C_comp          5.53197e-10  4.65065e-10  7.07186e-10 | CDL
C_comp_pullup    319e-12    NA        NA        | Measurement
C_comp_pulldown  232e-12    NA        NA        | Measurement
```

In case that large discrepancy appear in the total capacitance, need to regenerate IBIS model adding supplemental capacitance to the Spice netlist.

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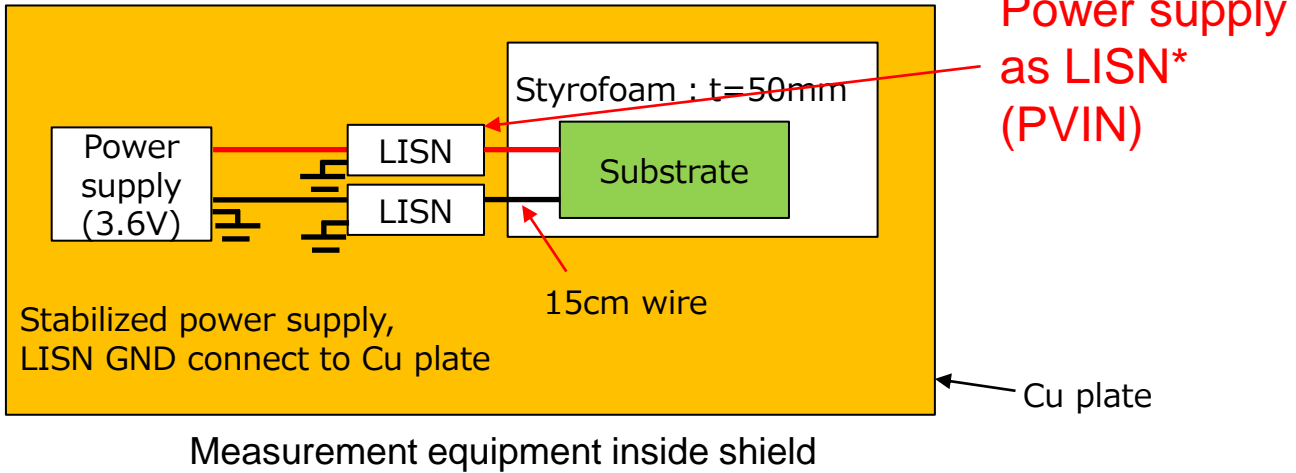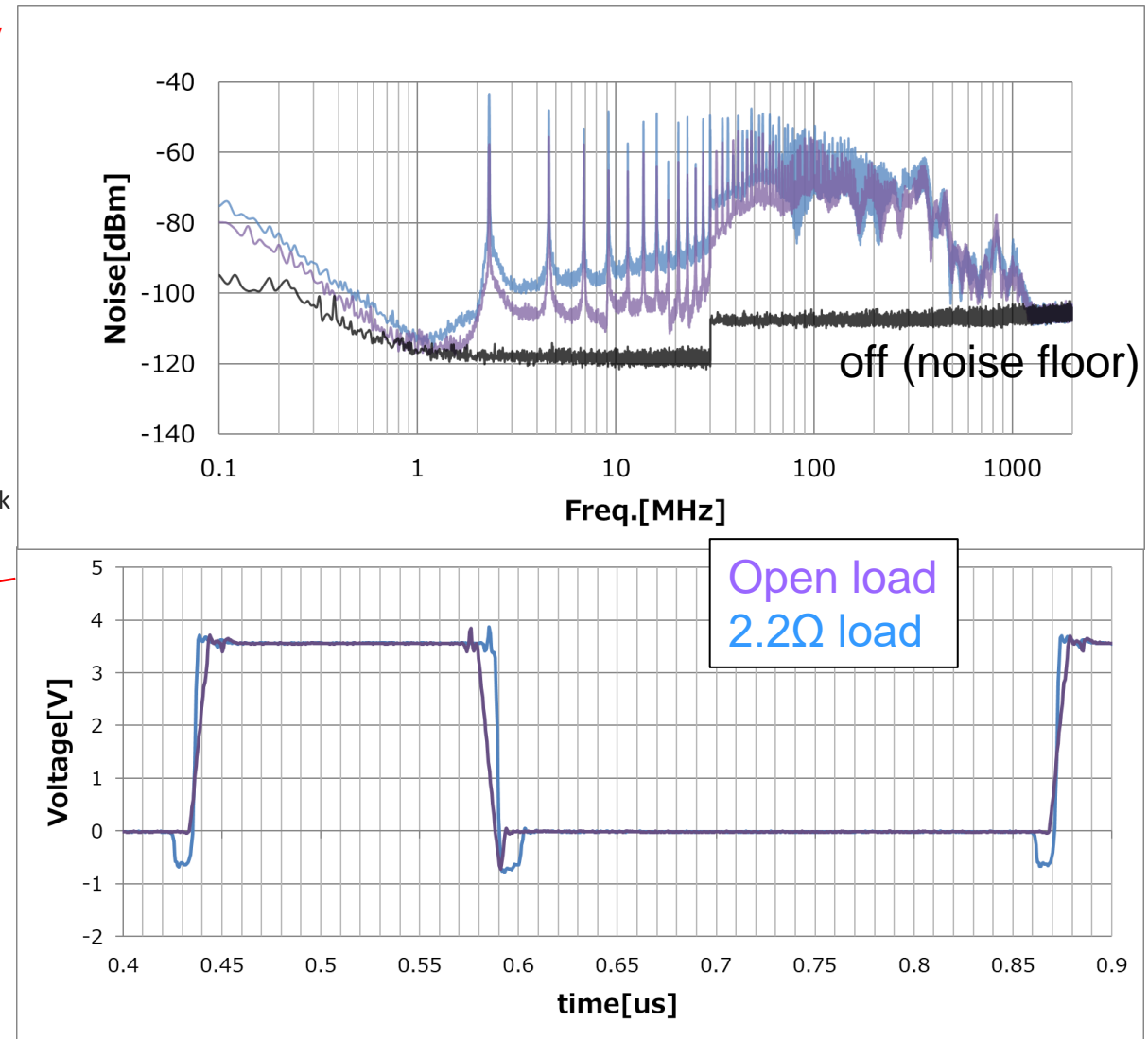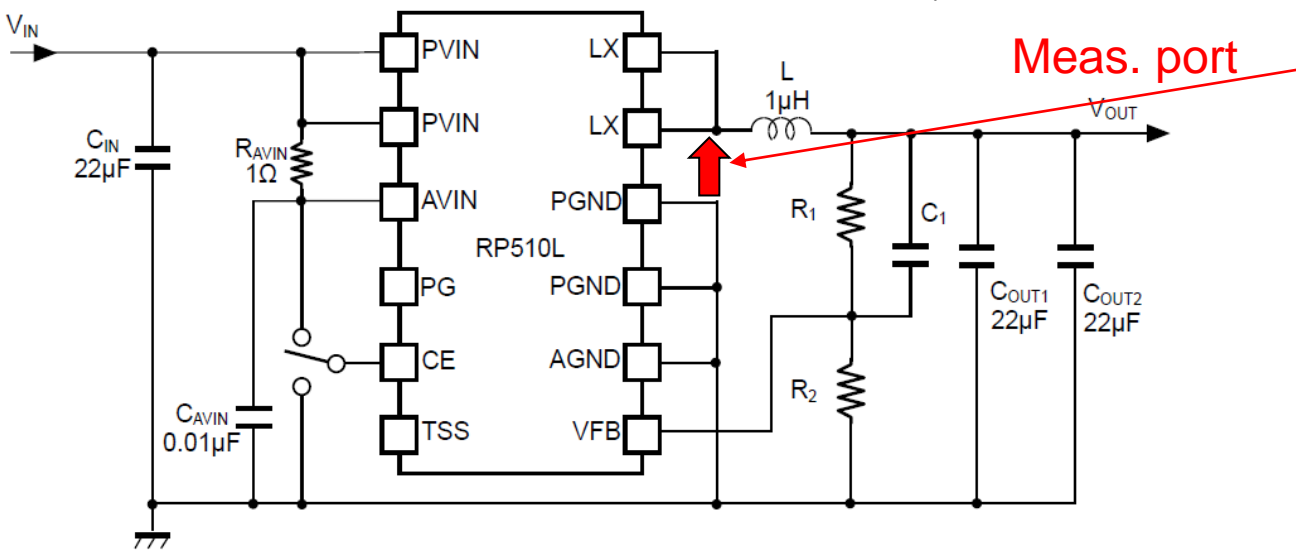# Measurement circuit construction

DUT

Evaluation board

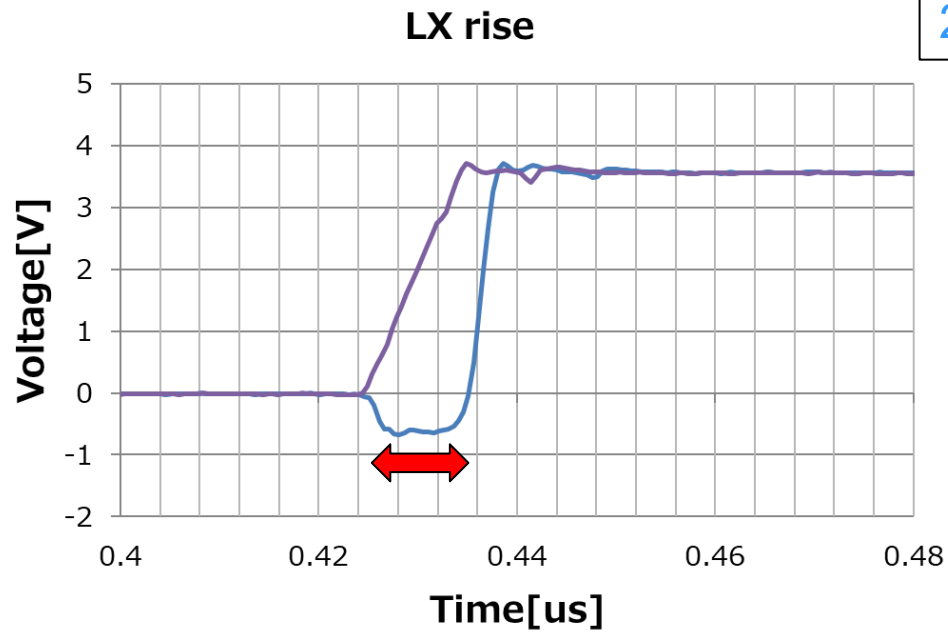Vout load
①Open
②2.2Ω

Measurement environment and results

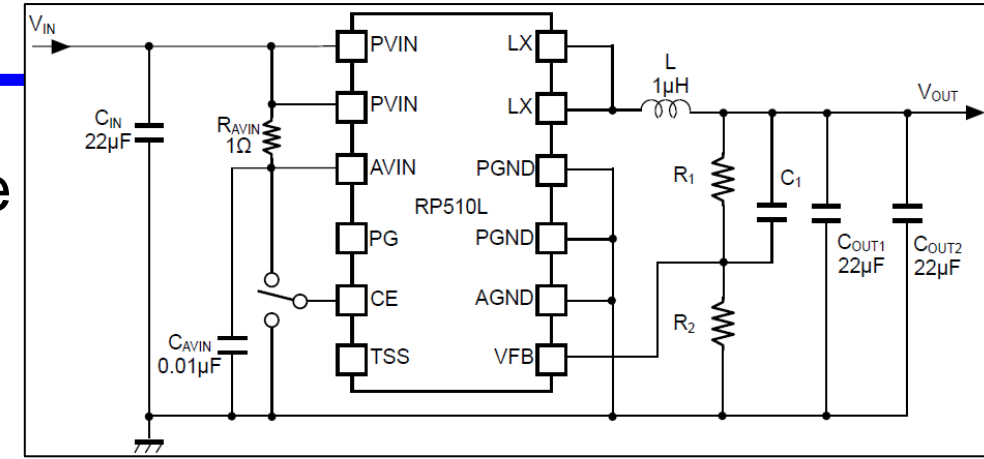
Power supply as LISN* (PVIN)

Styrofoam : t=50mm

Power supply (3.6V)

LISN

LISN

Substrate

15cm wire

Stabilized power supply, LISN GND connect to Cu plate

Cu plate

Measurement equipment inside shield

*LISN:Line Impedance Stabilization Network

off (noise floor)

Meas. port

Open load
2.2Ω load

V_{IN}

C_{IN} 22µF

R_{AVIN} 1Ω

C_{AVIN} 0.01µF

PVIN

PVIN

AVIN

PG

CE

TSS

RP510L

LX

LX

PGND

PGND

AGND

VFB

L 1µH

V_{OUT}

R_1

C_1

R_2

C_{OUT1} 22µF

C_{OUT2} 22µF

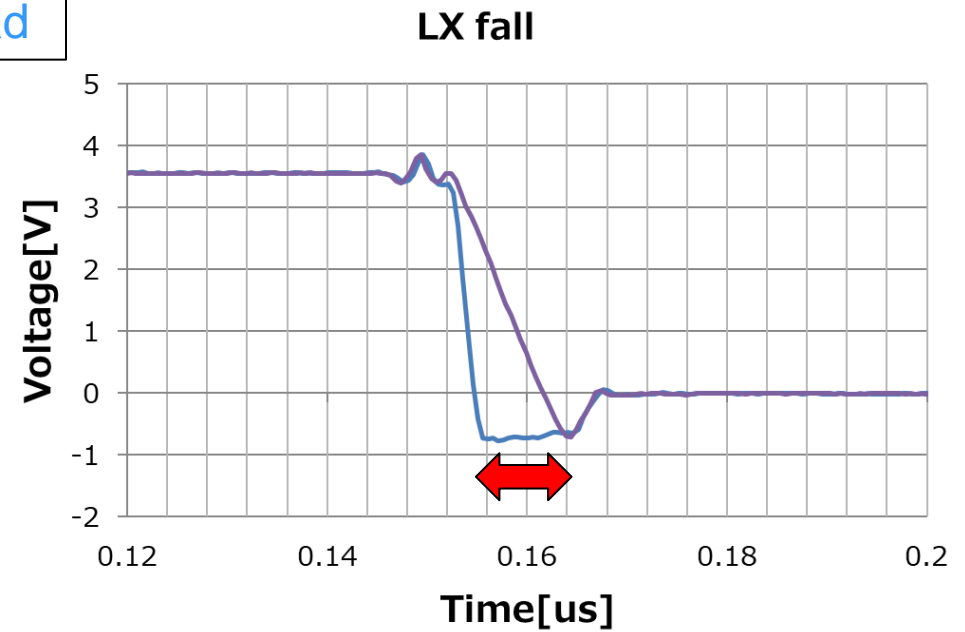# Measured LX waveform

Dead time appears in LX waveform with resistive load

Open load
2.2Ω load

LX rise

LX fall

Printed circuit board model

Modeling printed circuit board by electromagnetic analysis
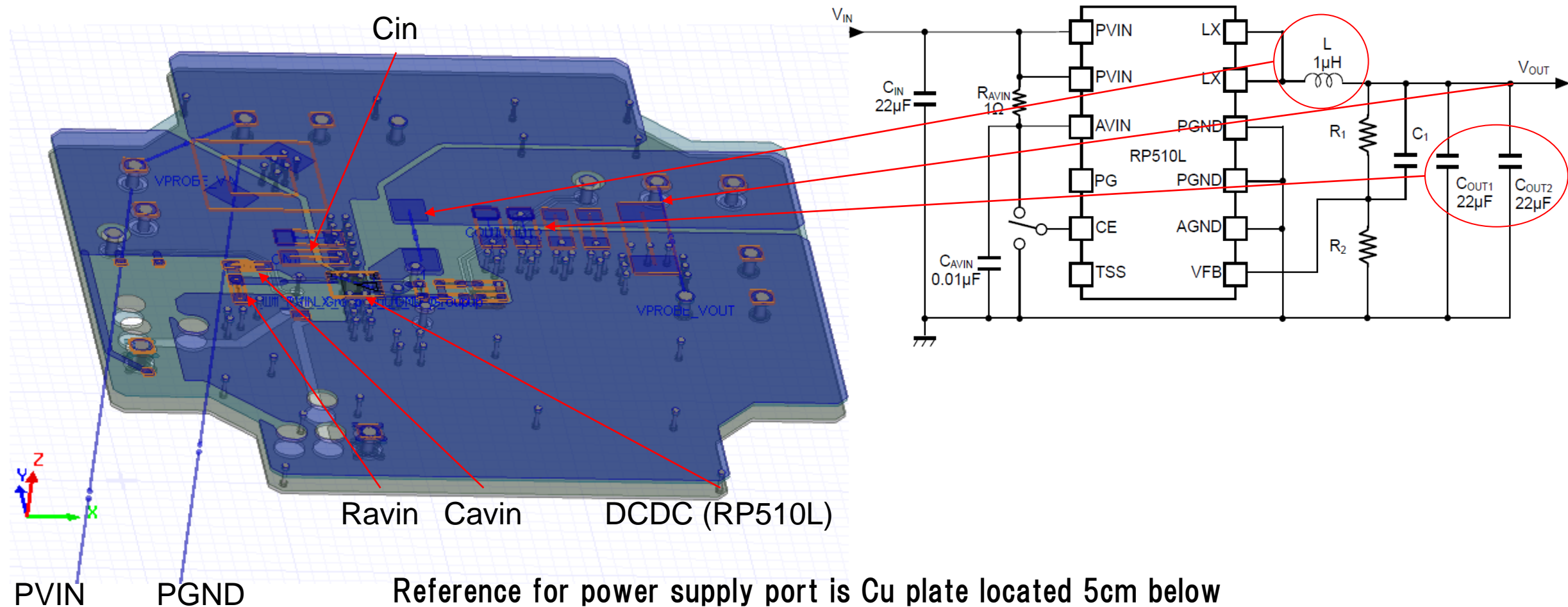
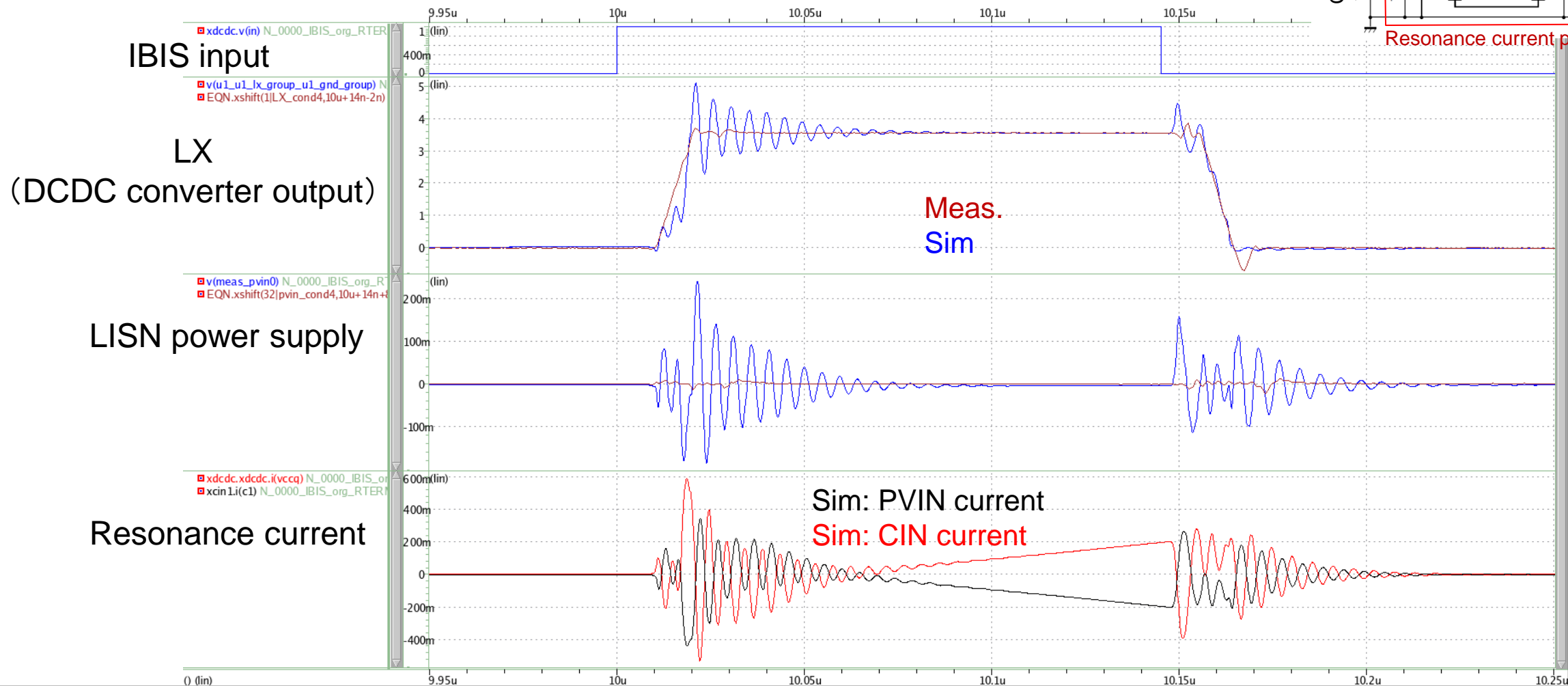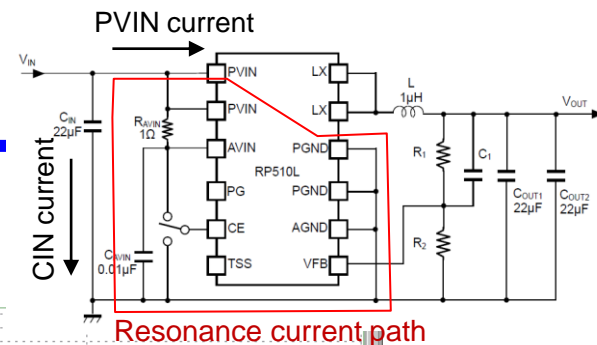Reference for power supply port is Cu plate located 5cm below

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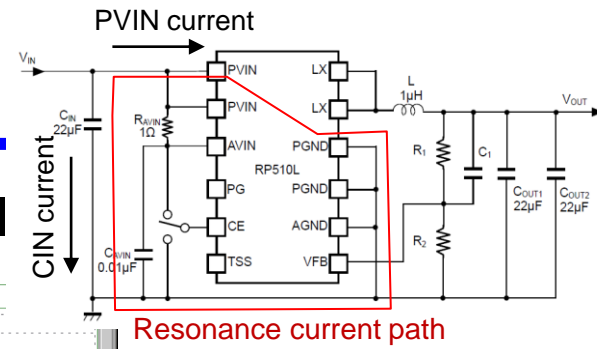- Summary
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Simulation results：Open

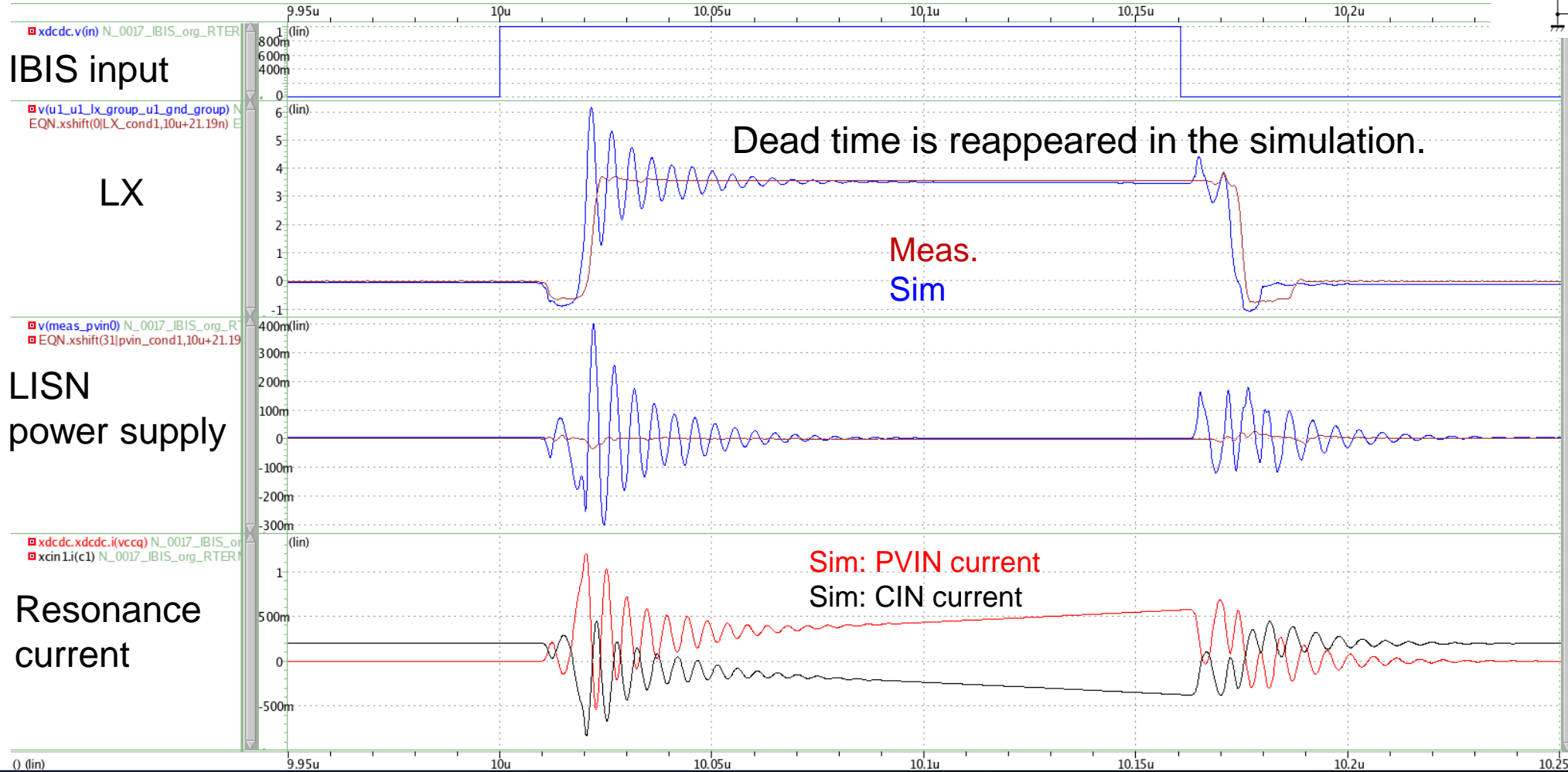Large ringing appears in the simulation results unlike measurements.

IBIS input

LX
（DCDC converter output）

Meas.
Sim

LISN power supply

Resonance current

Sim: PVIN current
Sim: CIN current

Simulation results：Resistive load

Large ringing appears in the simulation results unlike measurements, as well

Resonance current path

IBIS input

LX

Dead time is reappeared in the simulation.

Meas.
Sim

LISN power supply

Sim: PVIN current
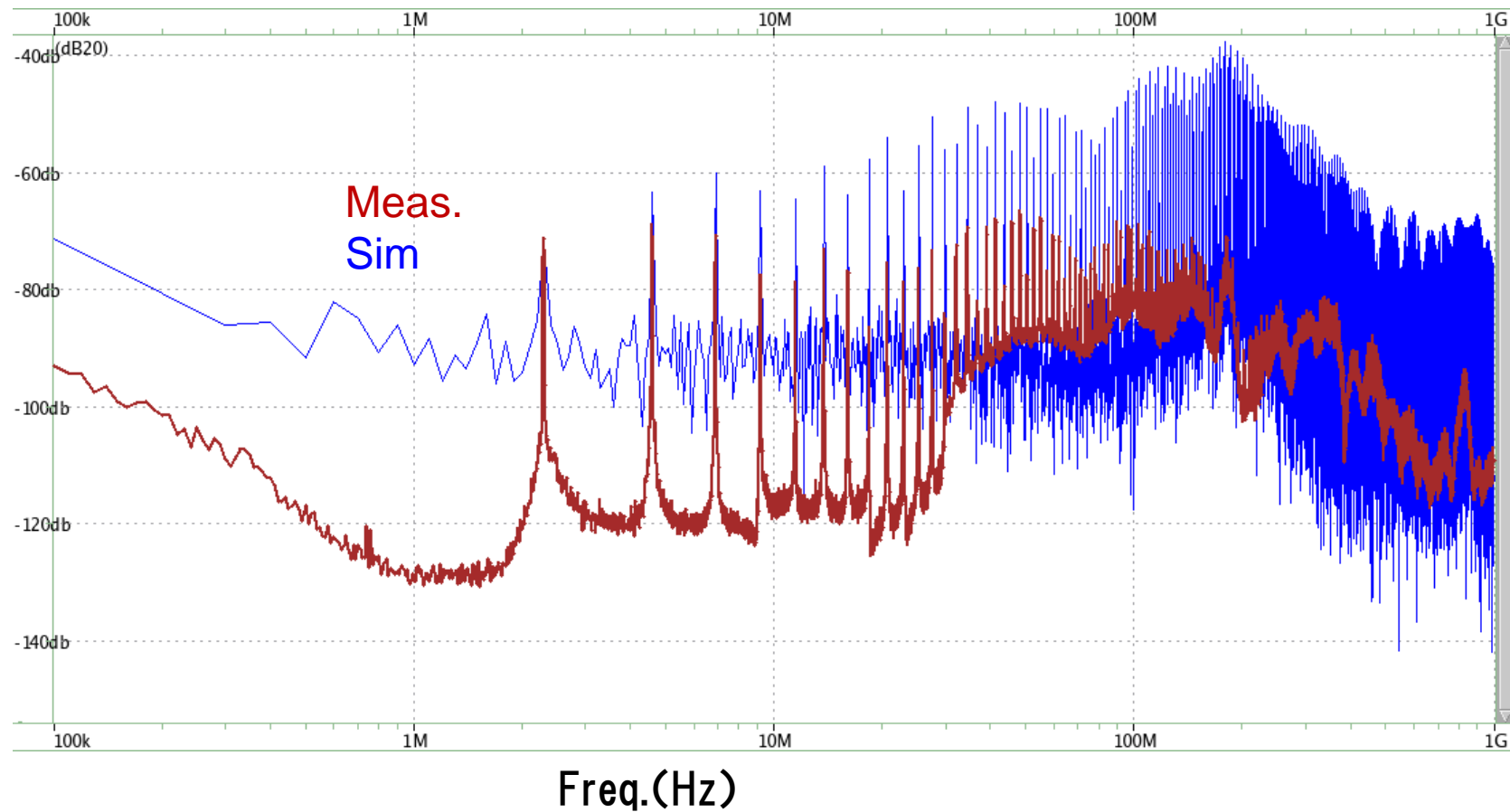Sim: CIN current

Resonance current

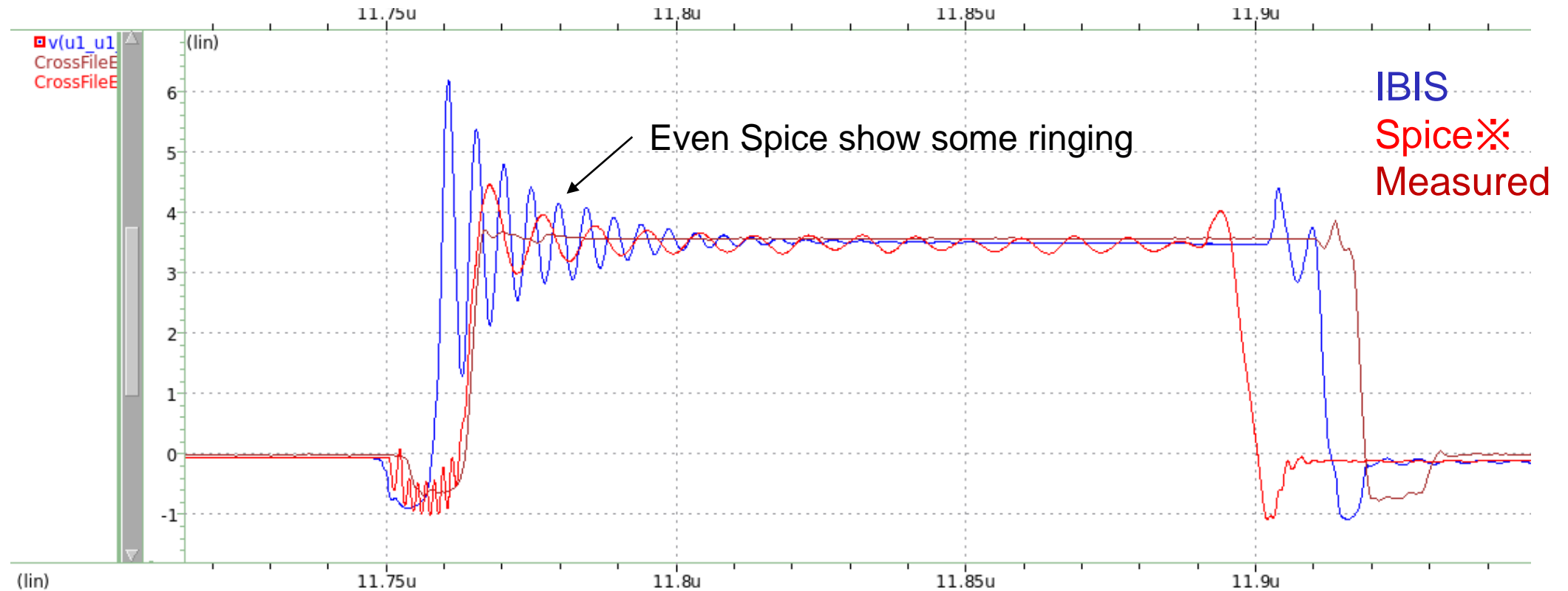Ringing caused by resonance current path through PVIN,PGND,CIN

CISPR25 (Voltage) PVIN Noise: Open load

The simulation is up to 30db larger than the measured

LX (Output) Voltage: Spice, IBIS vs. Measurement

Even Spice simulation show some ringing waveform
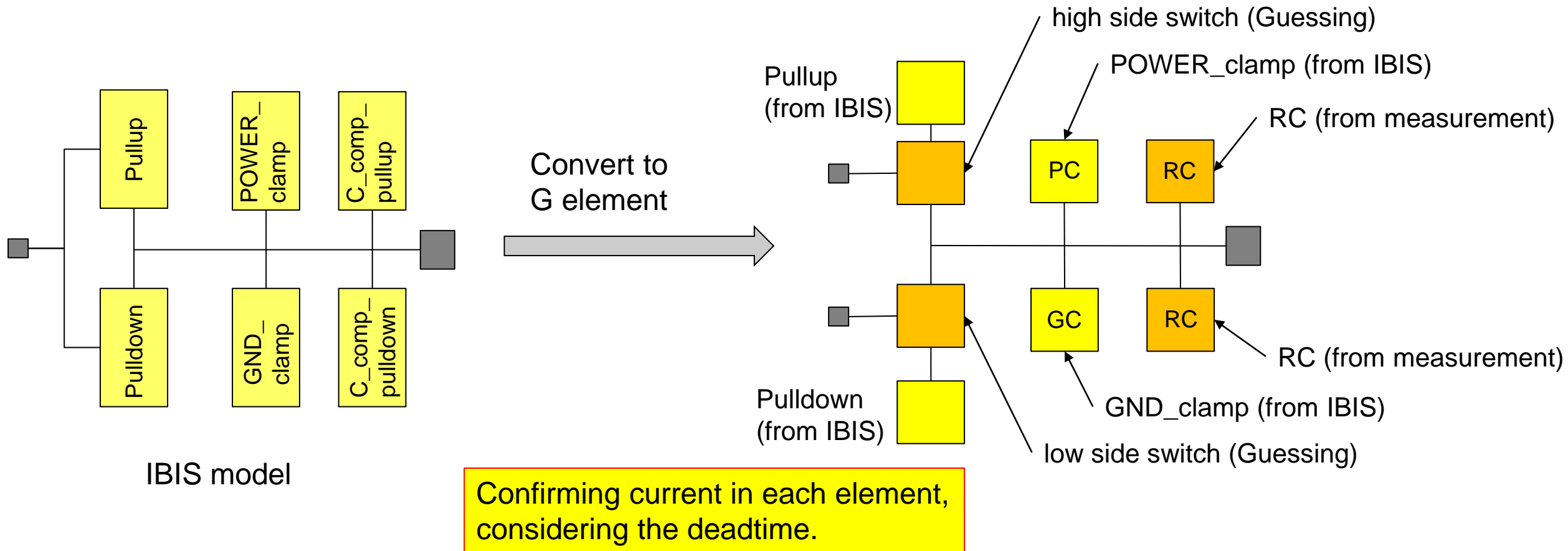After trying to eliminate the ringing, consider the JISSO modeling.

※With pre-layout Spice netlist

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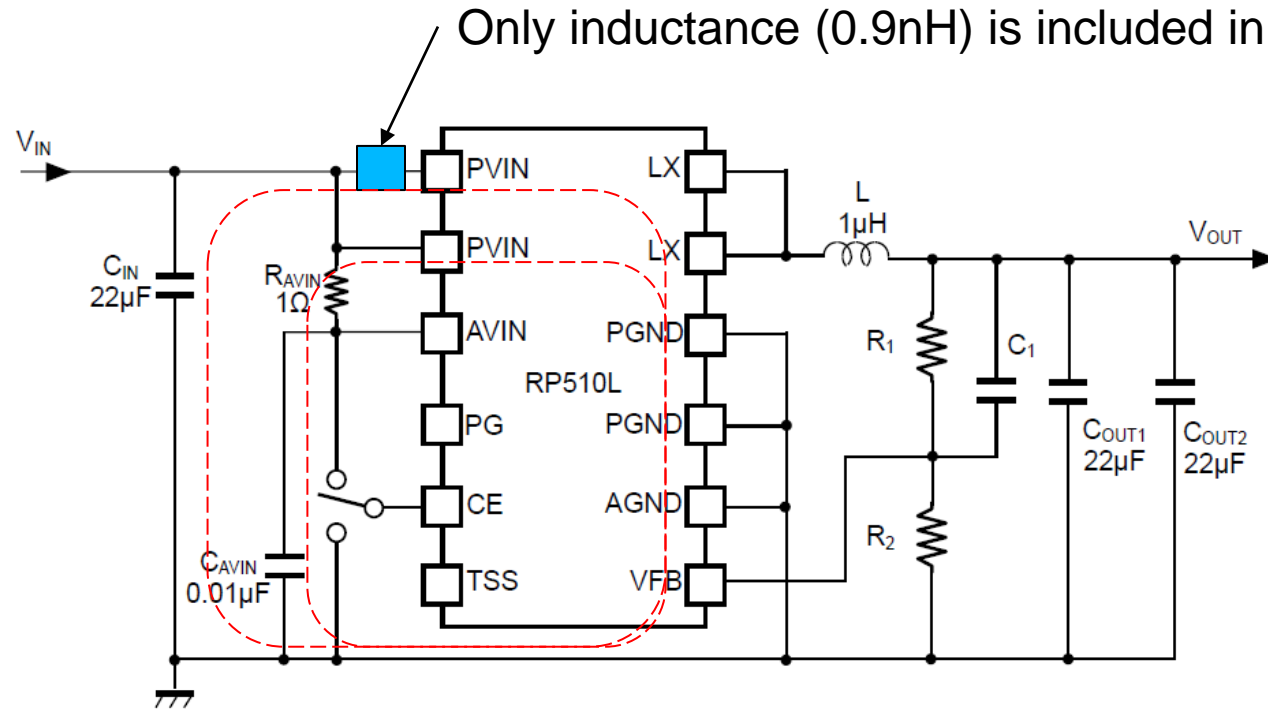- Summary

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From IBIS model to Spice macro-model

IBIS analysis by a circuit simulator is a black box approach. Not suitable for cause analysis.

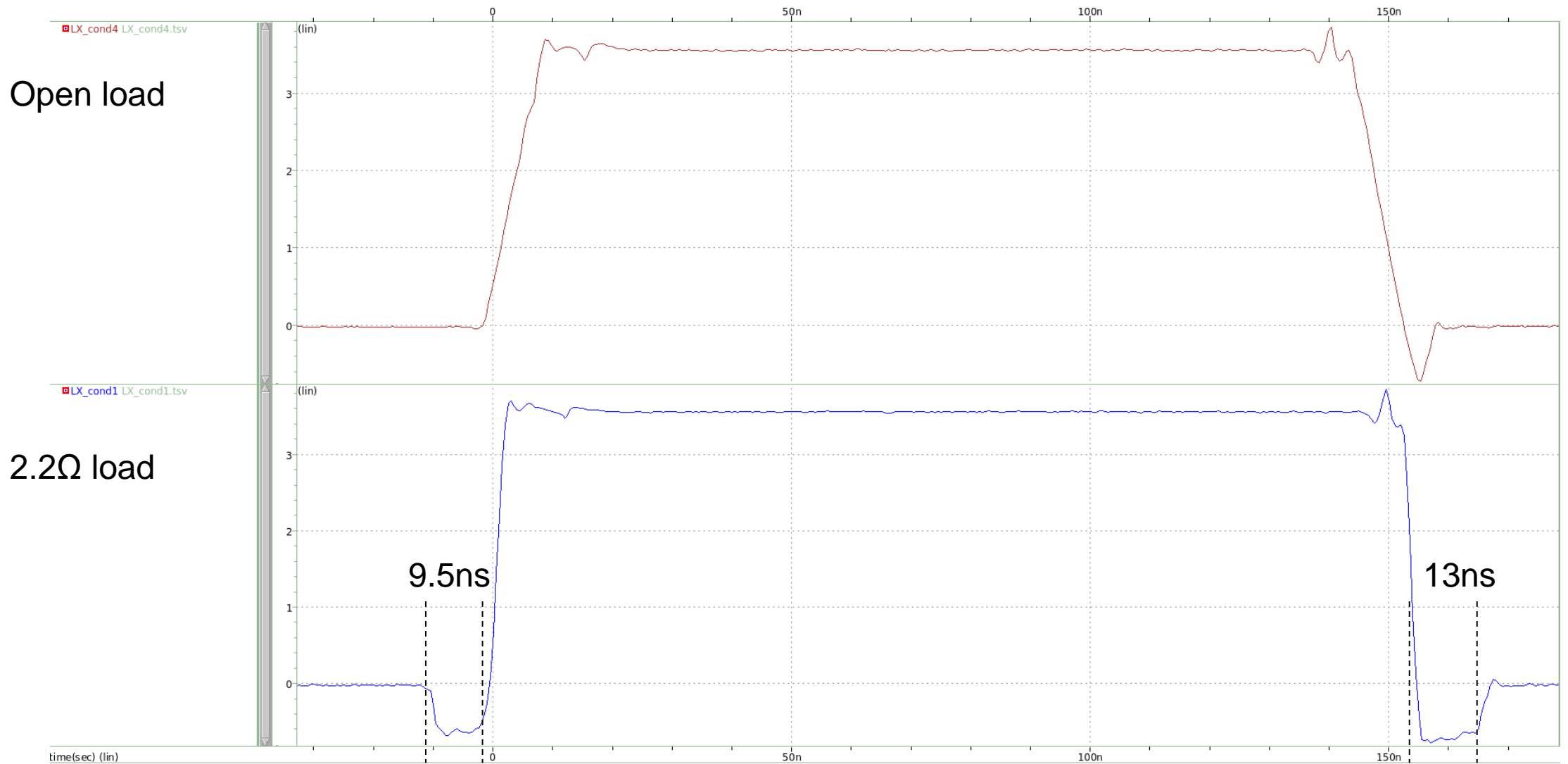Macro modeling replacing IV tables in IBIS with G element in Spice. Then, white box analysis.

IBIS model

Convert to G element

Pullup (from IBIS)

Pulldown (from IBIS)

high side switch (Guessing)

POWER_clamp (from IBIS)

RC (from measurement)

RC (from measurement)

GND_clamp (from IBIS)

low side switch (Guessing)

Confirming current in each element, considering the deadtime.

A simple implementation

To simplify, only PVIN inductance is converted from S-parameter
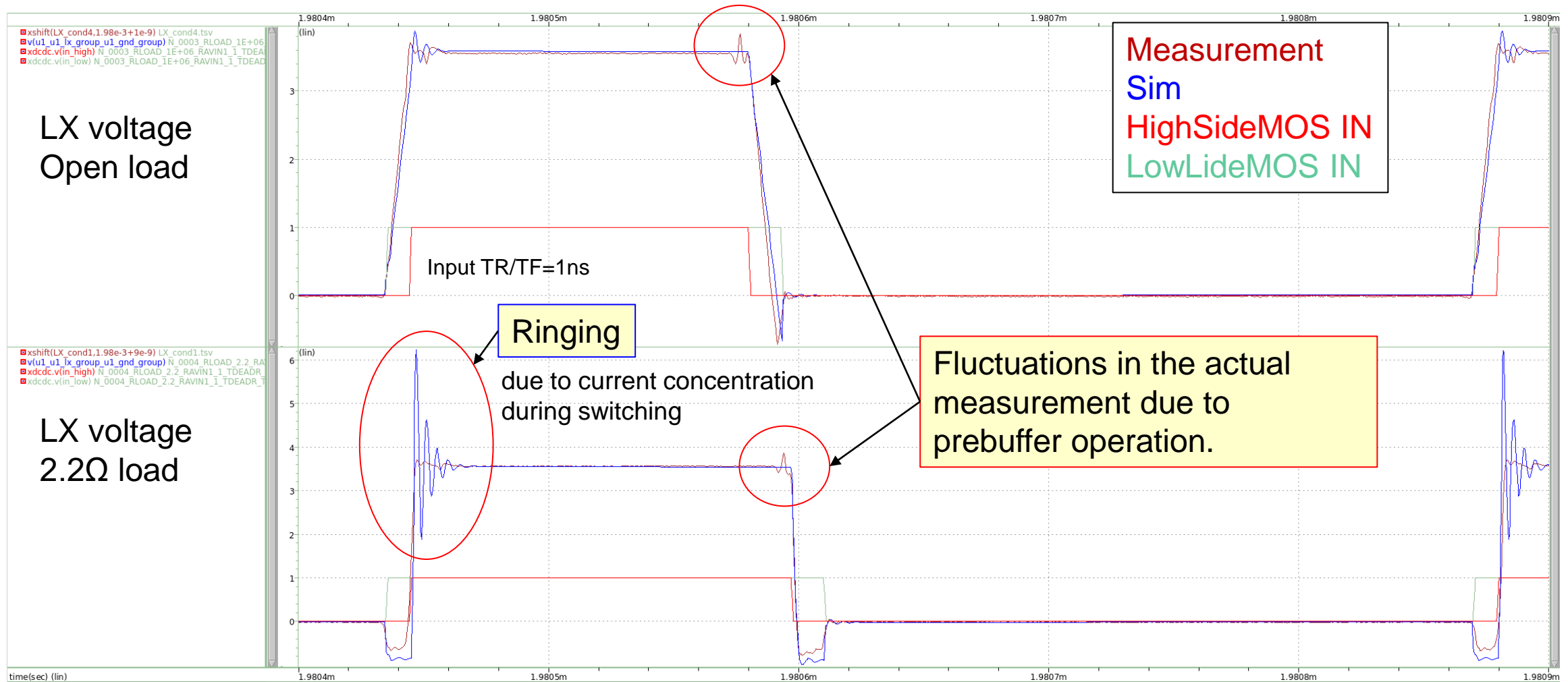
Only inductance (0.9nH) is included in the circuit to analyze.

From EM field solver
CIN loop inductance：0.88nH
CAVIN loop inductance：2.17nH

Estimating deadtime from measurement (LX voltage)

Open load

2.2Ω load

9.5ns

13ns

Simulation result of Spice macro model (Simplified)

LX voltage
Open load

LX voltage
2.2Ω load

Input TR/TF=1ns

Measurement
Sim
HighSideMOS IN
LowLideMOS IN

Ringing

due to current concentration
during switching

Fluctuations in the actual
measurement due to
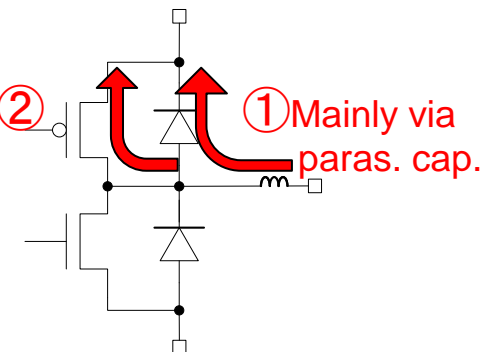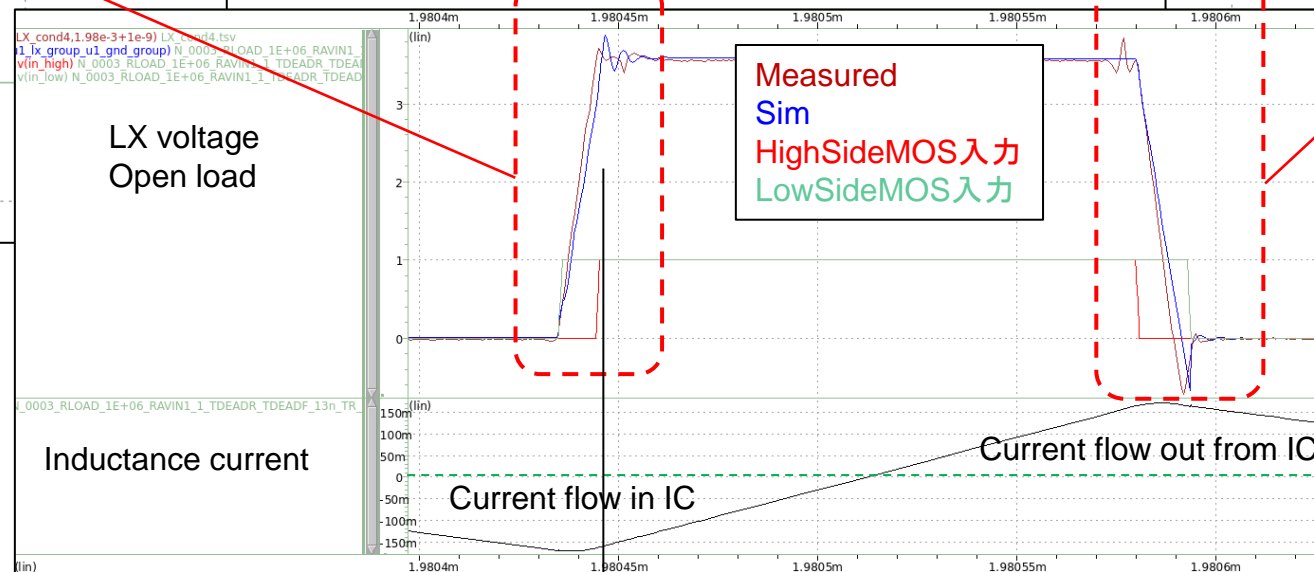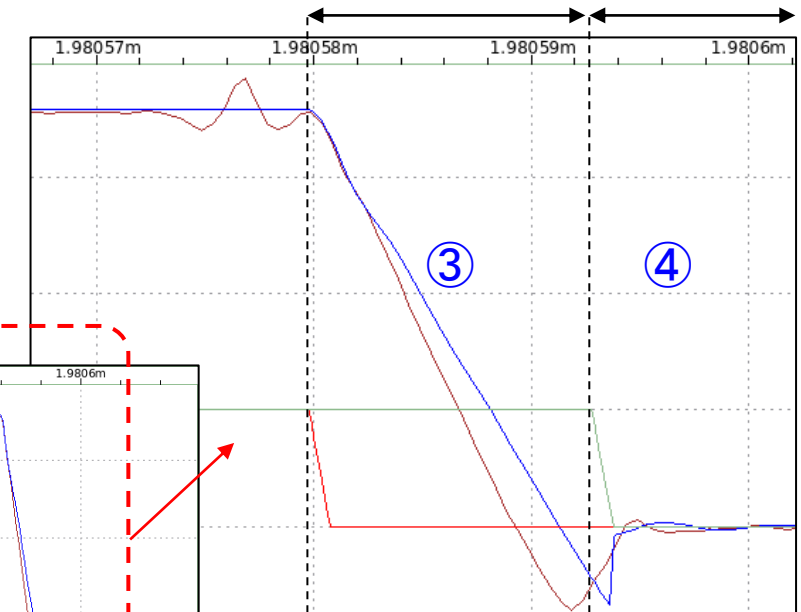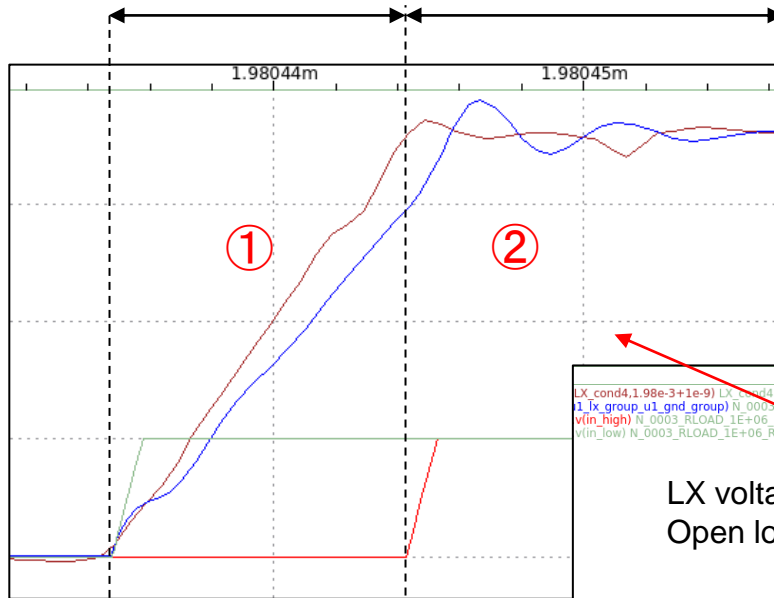prebuffer operation.

Discussion according to macro model (Open load)

During deadtime, HighSide body diode dominated characteristic

HighSideMOS char.

During deadtime, LowSide body diode dominated characteristic

LowSide MOS char.

①

②

③

④

LX voltage
Open load

Measured
Sim
HighSideMOS入力
LowSideMOS入力

Inductance current

Current flow out from IC

Current flow in IC

② ①Mainly via paras. cap.

④ ③Mainly via paras. cap.
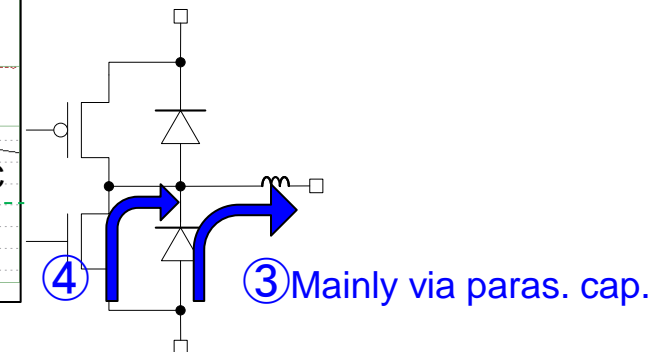
Discussion according to macro model (2.2Ω load)

During deadtime, HighSide body diode dominated characteristic

HighSideMOS char.

During deadtime, LowSide body diode dominated characteristic
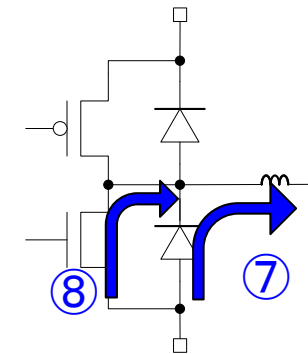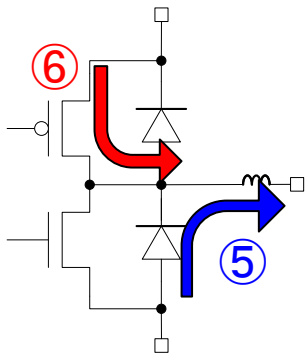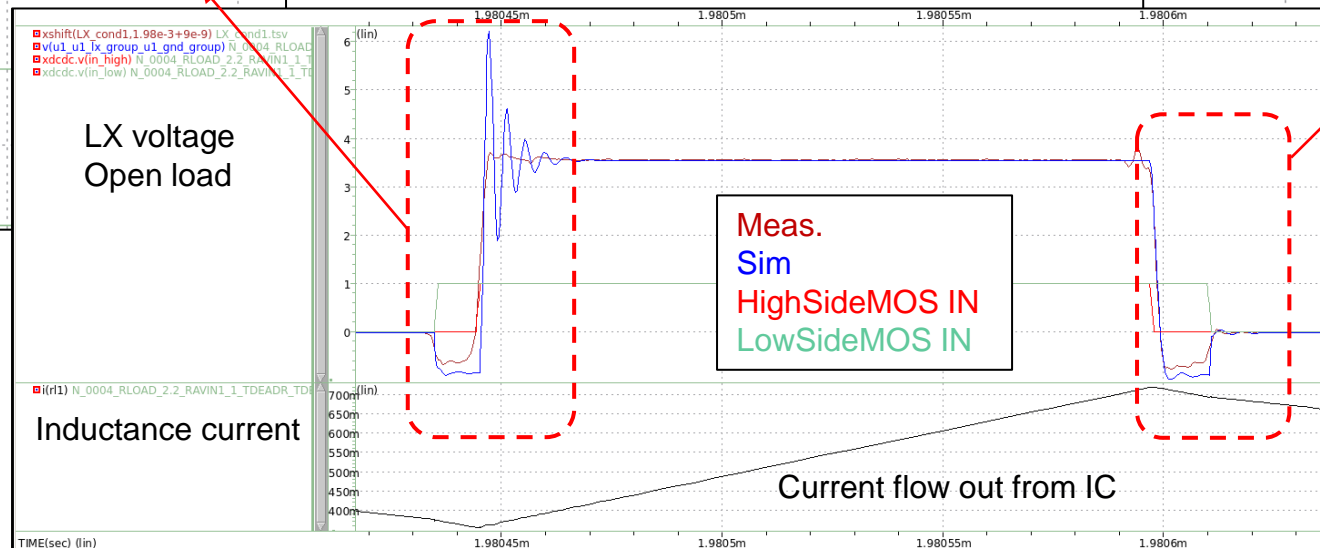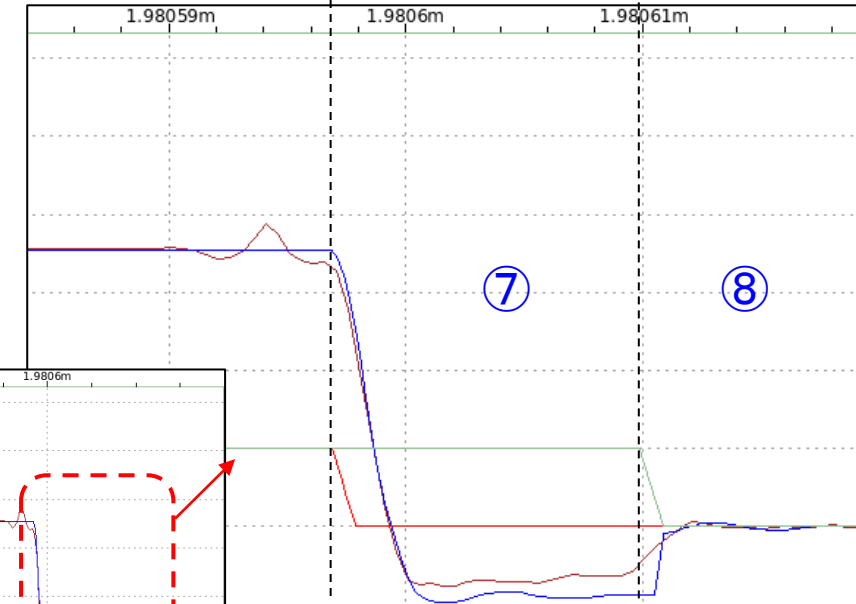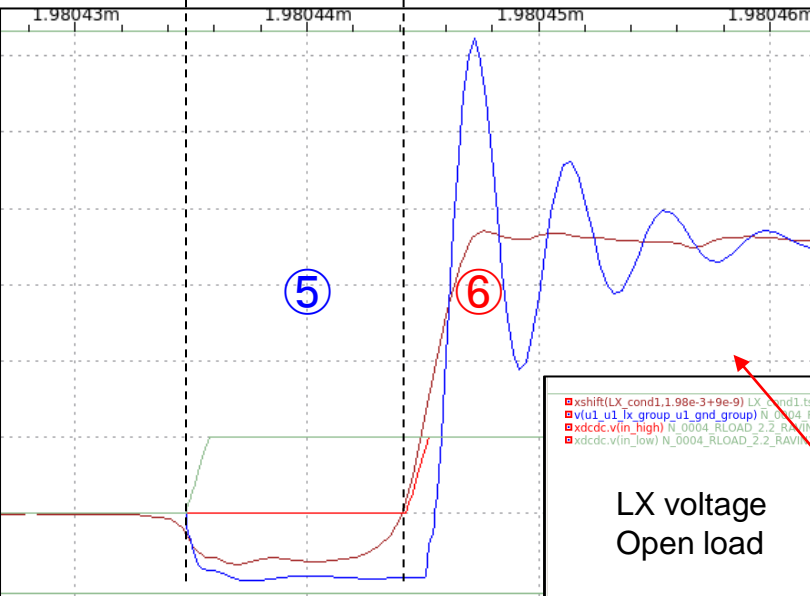
LowSide MOS char.

LX voltage
Open load

Inductance current

Meas.
Sim
HighSideMOS IN
LowSideMOS IN

Current flow out from IC

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Modified Spice macro model

The actual drivers were divided into

・HighSide： Small・Medium・Large transistors

・LowSide： Medium・Large transistors

Modified Spice macro model assuming
   HighSide: 10%,30%,60%
   LowSide： 40%,60%
RCs inserted considering post-layout

Considering post-layout situation distributes the operating timing, and then mitigates the unexpected current.

PVIN

10%   30%   60%

PC   RC

HighSide入力

LX

LowSide入力

GC   RC

40%   60%

PGND
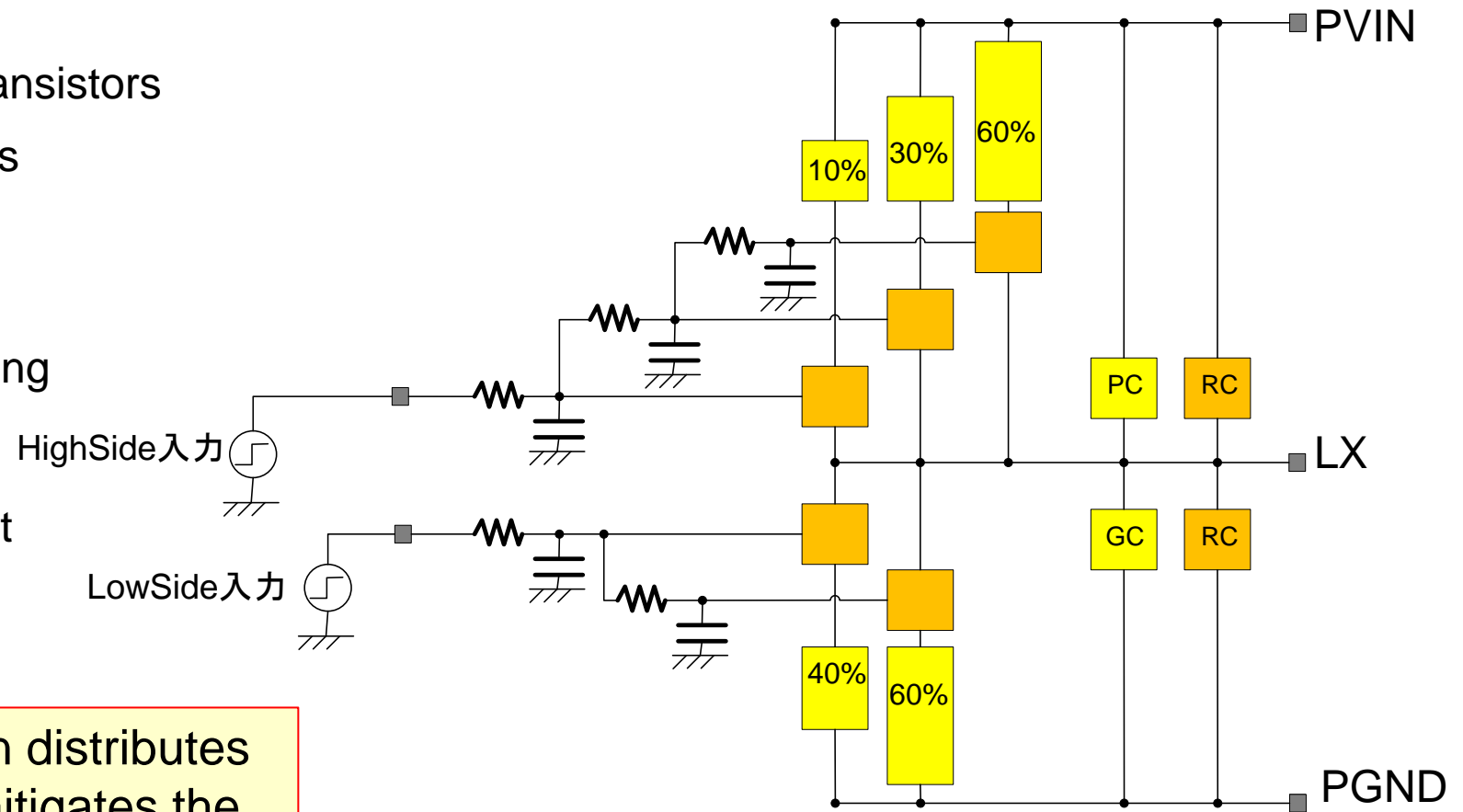
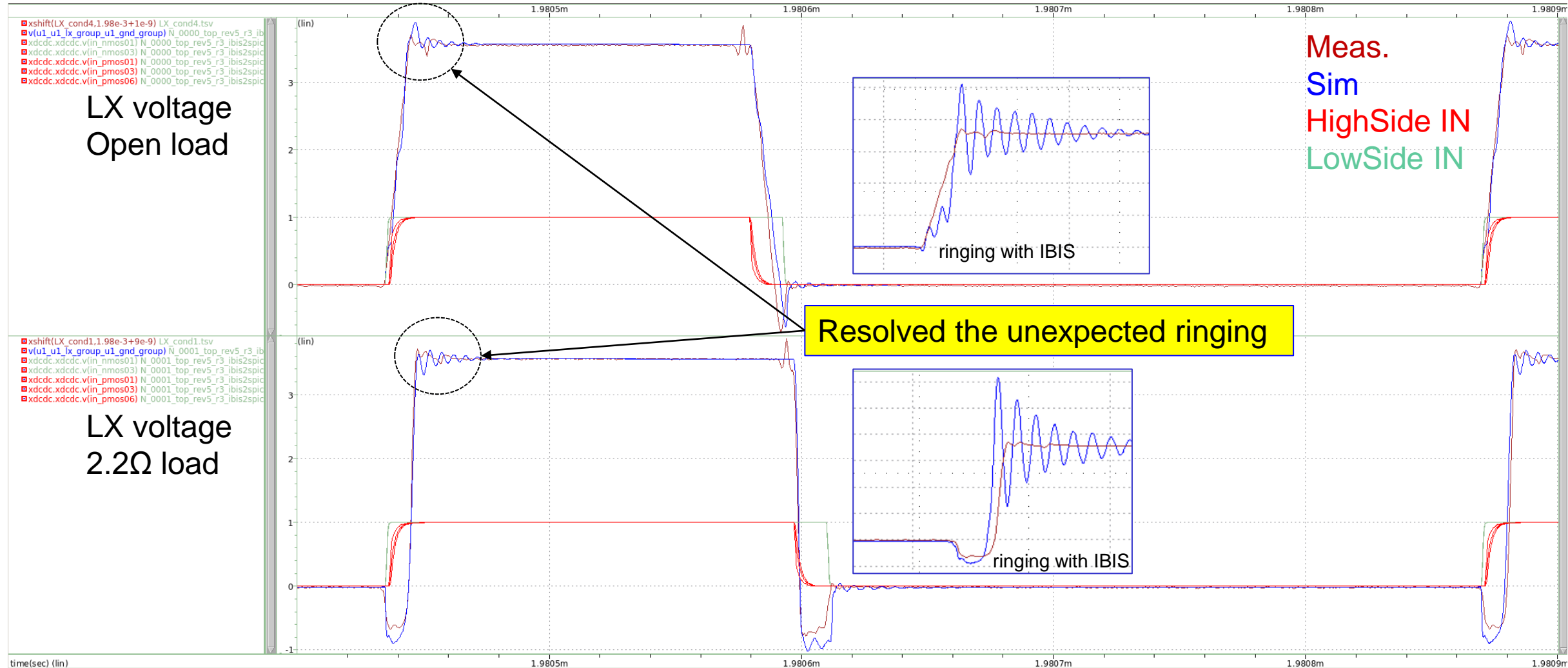Modified Spice macro model

Divided G-element by drivability, Inserted parasitic RCs

Modified Spice macro model results (Simplified)

LX voltage
Open load

Meas.
Sim
HighSide IN
LowSide IN

LX voltage
2.2Ω load

Resolved the unexpected ringing

Modified Spice macro model results (S-parameter)

LX voltage
Open load

LX voltage
2.2Ω load

Meas.
Sim
HighSide IN
LowSide IN

ringing with IBIS

ringing with IBIS

Resolved the unexpected ringing

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Summary

- Considering driver subdivisions as well as post-layout timing and slew rate is indispensable to re-create the actual waveform.

- In our experiment, adopting the actual driver subdivisions with the parasitic RC network has mitigated the previously reported unexpected current concentration and ringing in the waveform.

Remaining issue and future work

Remaining issue：

Organized extraction and modeling methods of the red dotted line surrounded part.

Macro-modeling of the pre-buffer resolves the issue, however tradeoff between effectiveness and confidentiality of the driver configuration.
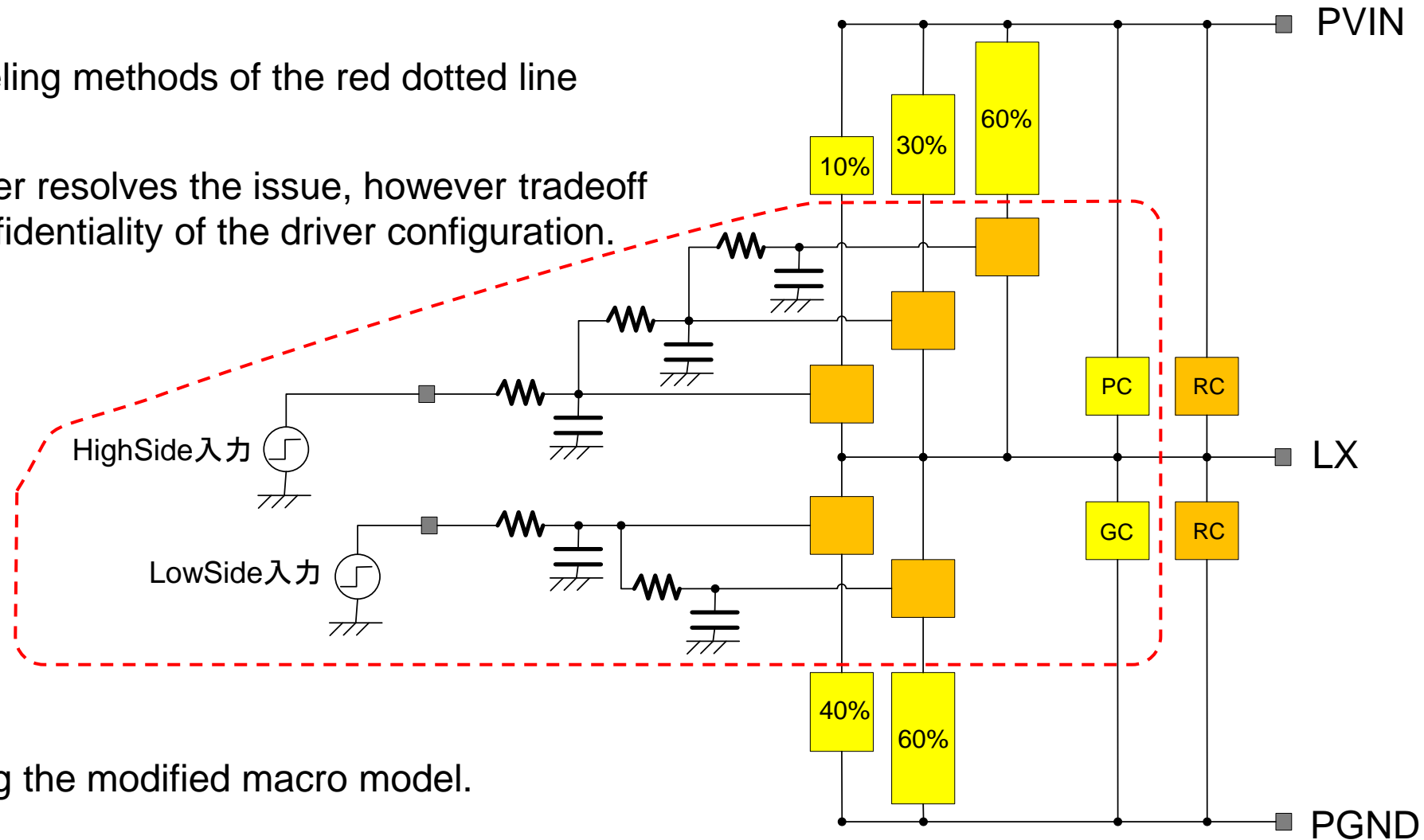
Future work：
CISPR25 EMI analysis utilizing the modified macro model.