

Asian IBIS Summit
Tokyo, JAPAN
November 13th, 2020

The On-Die Decoupling Capacitor Model (BIRD198.3)

JEITA

Semiconductor & System design technical committee
LSI Package Board Interoperable Design Subcommittee
Model Based / Systems Design Working Group

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BIRD 198 is Ready !

- March 11, 2019 BIRD198
- April 3, 2020 BIRD198.1
- June 23, 2020 BIRD198.2
- August 7, 2020 BIRD198.3 **Accepted**

– <https://ibis.org/birds/>

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
207	New AMI Reserved Parameters Component Name and Signal Name	Randy Wolff, Micron Technology	July 29, 2020		
206	Clarification of text "transition time"	Hansel Desmond Dsilva, Achronix Semiconductor; Walter Katz, Signal Integrity Software; Fangyi Rao, Keysight; Todd Bermensolo, Keysight; Arpad Muranyi, Mentor Graphics.	June 26, 2020		
205	New AMI Reserved Parameter for Sampling Position in AMI_Init Flow	Hansel Desmond Dsilva, Achronix Semiconductor; Walter Katz, Signal Integrity Software; Todd Bermensolo, Keysight; Fangyi Rao, Keysight; Arpad Muranyi; Mentor Graphics; Ambrish Varma, Cadence	May 14, 2020	June 26, 2020	
204	DQ_DQS GetWave Flow for Clock Forwarding Modeling	Walter Katz, The MathWorks Fangyi Rao, Keysight Wendem Beyene, Intel Ambrish Varma, Cadence	April 22, 2020	June 26, 2020	
203	Submodel Clarification	Randy Wolff, Micron Technology	March 10, 2020	April 24, 2020	
202	Electrical Descriptions of Modules	Walter Katz, Signal Integrity Software	January 22, 2020		
201.1	Back-channel Statistical Optimization	Walter Katz, Signal Integrity Software	January 7, 2020, June 2, 2020	July 17, 2020	
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx Receiver Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198.3	Keyword Additions for On-Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Sony LSI Design Inc.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiaki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019, April 3, 2020, June 23, 2020, August 7, 2020	August 7, 2020	

Agenda

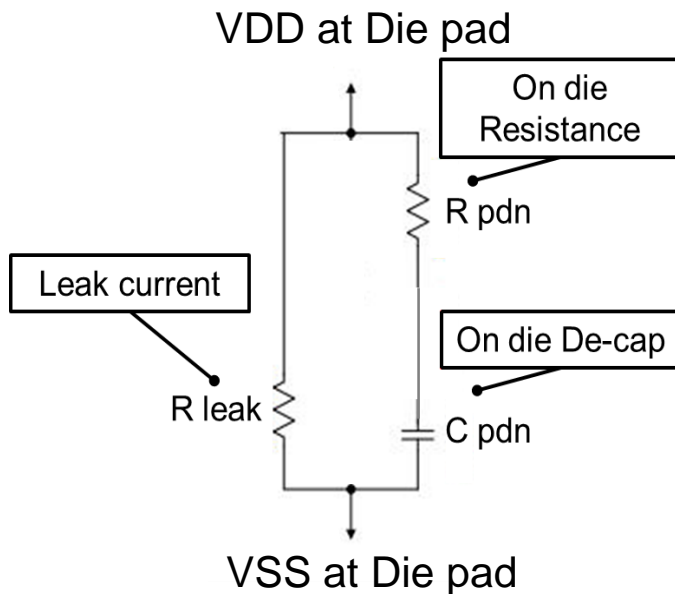
- Basics of On-Die PDN Model
- Examples
- Proposal to Chip Vendors
- Conclusion

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- Basics of On-Die PDN Model
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On-Die PDN Model

- On-Die Power Distribution Network (PDN) Model
 - Simple RC path between power and GND die pad
- New Keywords: [PDN Domain] and [PDN Model]



```
[Component] AAA
  [PDN Domain] PDN_for_VDD
  Bus_label VDD
  Bus_label VSS
  [PDN Model] VDD_decap
    C_pdn 5.1n 4.8n 5.2n
    R_pdn 0.1 0.15 0.05
    R_leak 15k 17k 11k
  [End PDN Model]
[End PDN Domain]
```

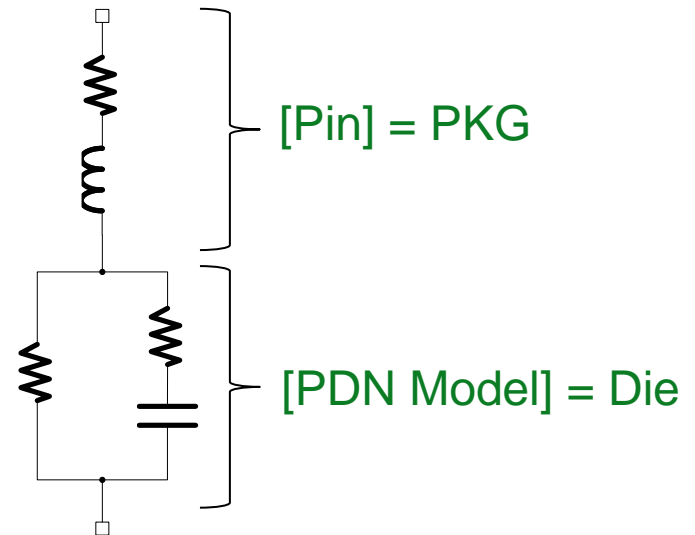
Concept is 'Simple Model'

- [PDN Model] is **very simple**

- Actual chip has more complex characteristic

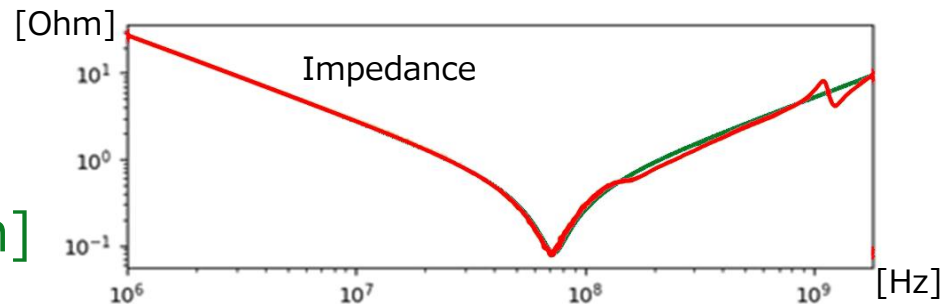
- Benefit

- Stable and fast simulation
- Human friendly
- What-if analysis
- Concealing actual circuit



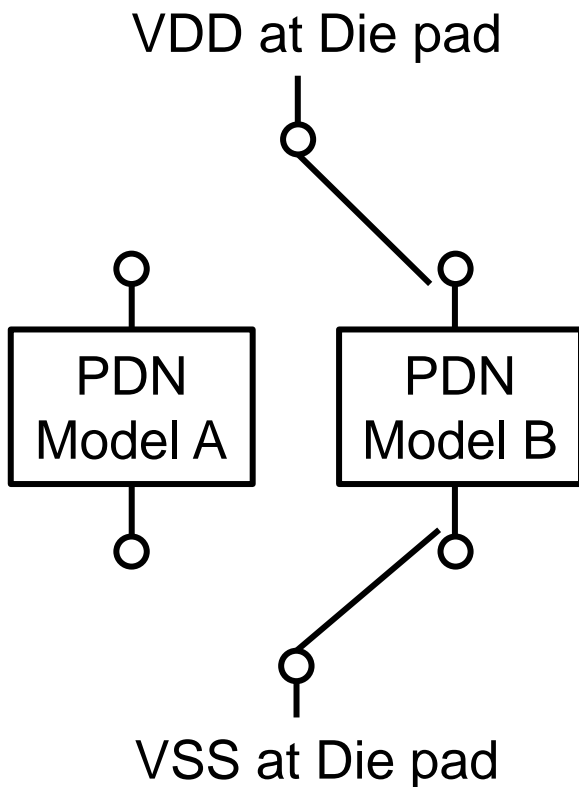
- Accuracy

- Measurement result
- [PDN Model] and [Pin]



Model Selecting Function

- Can select one [PDN Model] from multiple models
 - Vary RC value according to the operation mode



```
[Component] AAA
[PDN Domain] PDN_for_DDRCOMBOPHY
Bus_label VDD
Bus_label VSS
[PDN Model] VDD_DDR3mode
C_pdn 5.1n 4.8n 5.2n
R_pdn 0.1 0.15 0.05
R_leak 15k 17k 11k
[End PDN Model]
[PDN Model] VDD_DDR4mode
C_pdn 4.8n 4.5n 5.0n
R_pdn 0.1 0.15 0.05
R_leak 15k 17k 11k
[End PDN Model]
[End PDN Domain]
```

Variation Selecting Function

- [PDN Model] has PVT variation like any other IBIS keywords
 - These three value are called typ, min and max
- In [PDN Model], the order of values does **NOT** depend on magnitude

EDA Tool
select = 'min' → min column is selected, but the value is not necessarily minimum.

[PDN Model]	Decap		
C_pdn	5.1n	4.8n	5.2n
R_pdn	0.1	0.15	0.05
R_leak	15k	17k	11k

[End PDN Model]

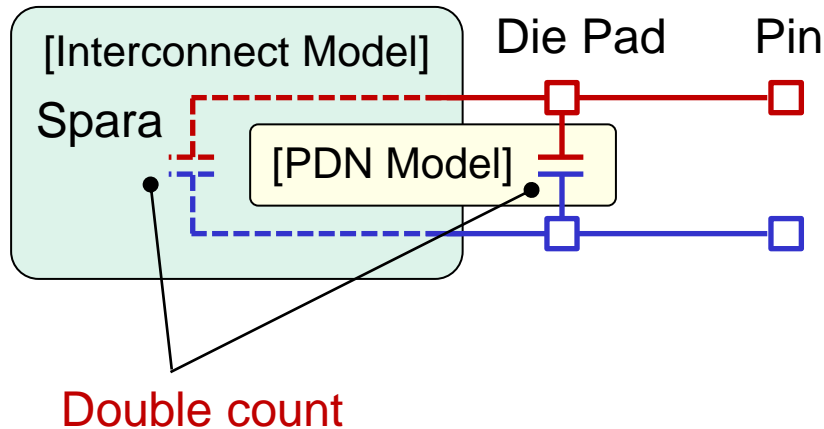
[Interconnect Model]

- [Interconnect Model] can also represent On-Die PDN
 - Difference between [PDN Model] and [Interconnect Model] corresponds to the difference between [Package]'s RLC and S-parameter

	[PDN Model]	[Interconnect Model]
On-Die PDN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
On PKG PDN	N/A	<input checked="" type="checkbox"/>
per Pad model	N/A	<input checked="" type="checkbox"/>
Model Selectable	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Variation Selectable	<input checked="" type="checkbox"/>	N/A
Format	Simple RC	S-para or SPICE
Usage	Only On-Die PDN	Not Only On-Die PDN

Cautionary points when using together

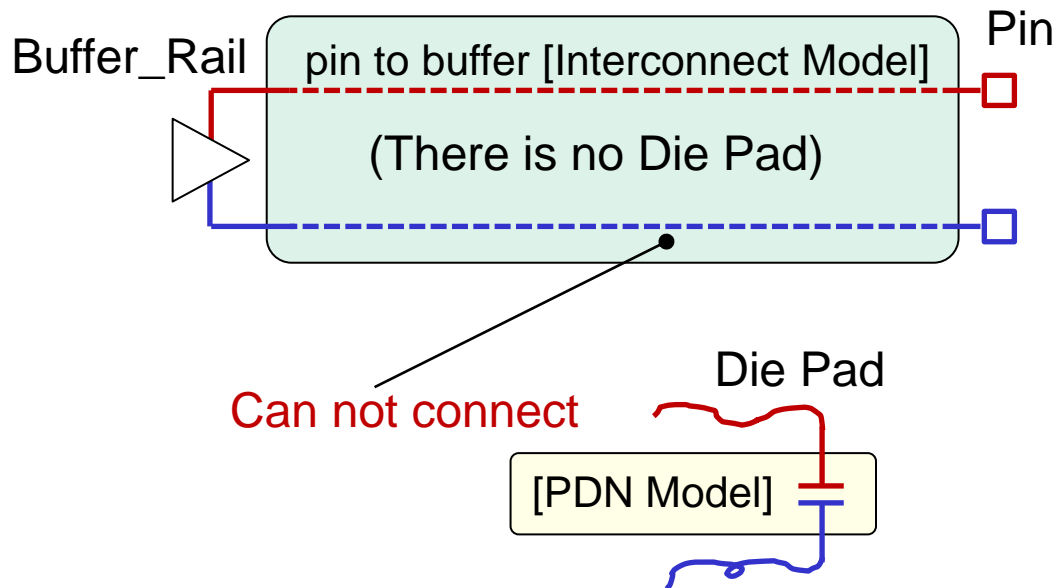
- Model maker should ensure that On-Die PDN characteristics are **not double counted**



```
[Interconnect Model] PDN_spara
File_TS aaa.s2p
Number_of_terminals = 3
1 Pad_Rail bus_label VDD
2 Pad_Rail bus_label VSS
3 Pad_Rail bus_label GND
[End Interconnect Model]
...
[PDN Domain] PDN_for_VDD
Bus_label VDD
Bus_label VSS
[PDN Model] Decap
...
[End PDN Model]
[End PDN Domain]
```

Cautionary points when using together

- [Interconnect Model] for pin to buffer does not have die pad interfaces, there is no connection with [PDN Model]



```
[Interconnect Model] PDN_spara
File_TS xxx.s4p
Number_of_terminals = 5
1 Pin_Rail bus_label VDD
2 Pin_Rail bus_label VSS
3 Buffer_Rail bus_label VDD
4 Buffer_Rail bus_label VSS
5 Pin_Rail bus_label GND
[End Interconnect Model]
...
[PDN Domain] PDN_for_VDD
Bus_label VDD
Bus_label VSS
[PDN Model] Decap
...
[End PDN Model]
[End PDN Domain]
```

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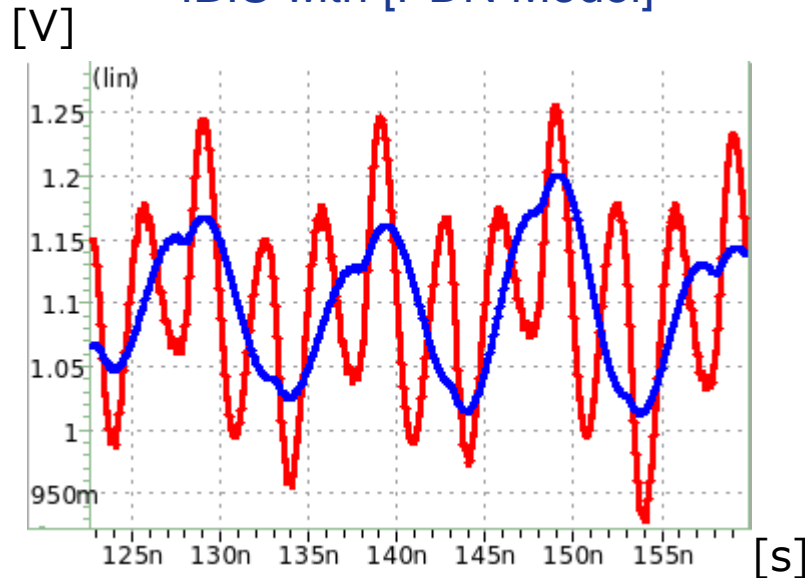


Example 1: LPDDR4 with SSN

■ Simulation result with and without [PDN Model]

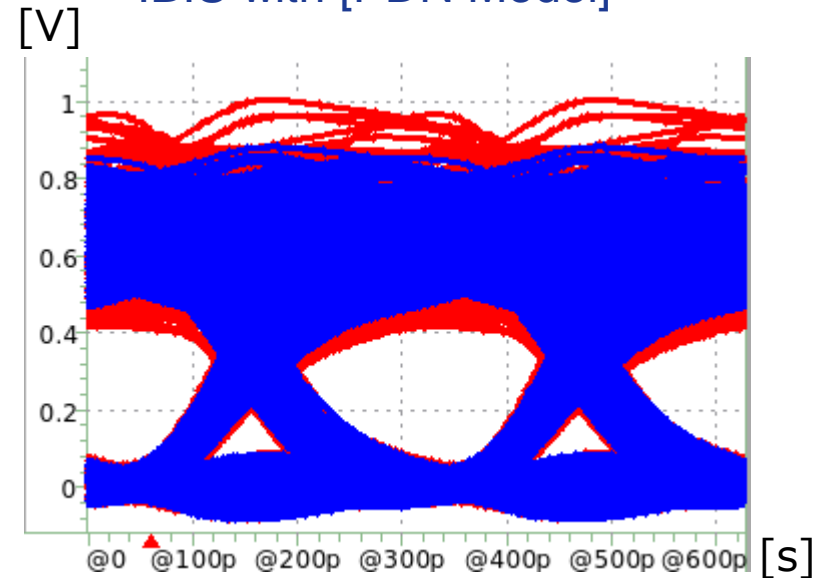
IO switching VDD noise at DIE

IBIS without [PDN Model]
IBIS with [PDN Model]



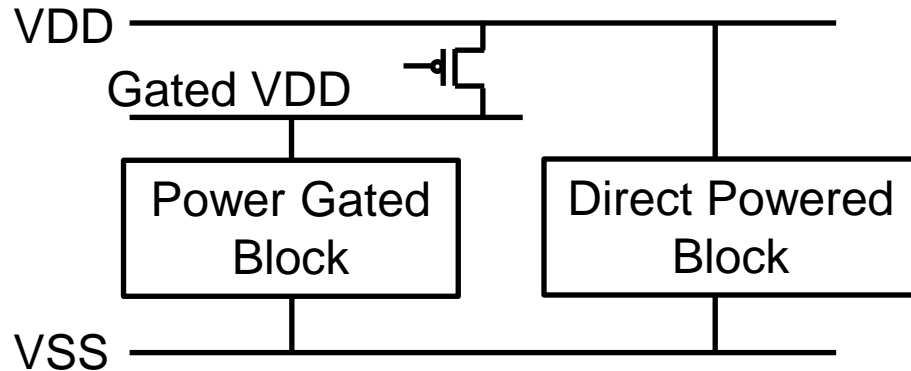
DQ Eye pattern at DRAM

IBIS without [PDN Model]
IBIS with [PDN Model]



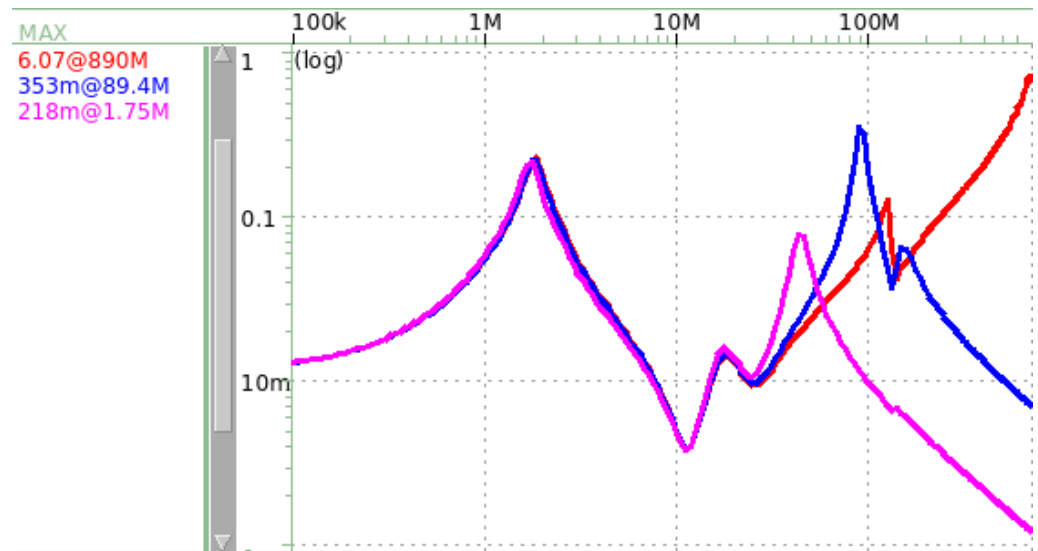
Example 2: Power Gating

■ Simulation result with and without [PDN Model]



PDN Input Impedance at DIE
IBIS without [PDN Model]
IBIS with [PDN Model] Gate_OFF
IBIS with [PDN Model] Gate_ON

```
[PDN Domain] VDD_core
Bus_label VDD
Bus_label VSS
[PDN Model] Gate_OFF
  C_pdn  32n  30n  37n
  R_pdn  7m   8m   6m
  R_leak 15k  17k  14k
[End PDN Model]
[PDN Model] Gate_ON
  C_pdn  185n 178n 193n
  R_pdn  5m   6m   5m
  R_leak 10k  13k  9k
[End PDN Model]
[End PDN Domain]
```

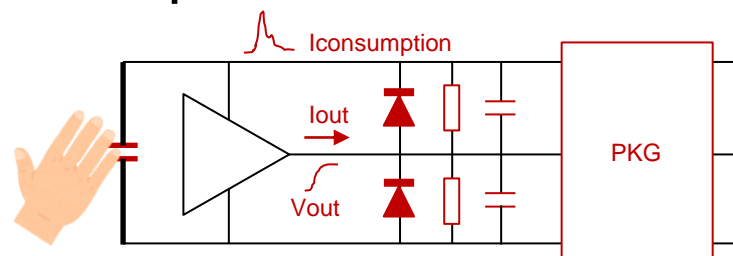


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Need for [PDN Model]

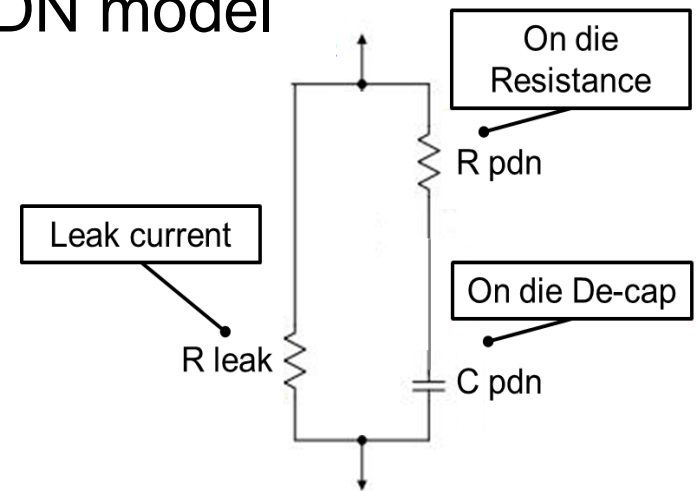
- IBIS already includes critical information
 - Output current, Output waveform, Consumption current waveform, ESD protection diode characteristics, On die termination characteristics, Signal pad capacitance, PKG, etc.



- **What do you conceal On-Die PDN model for ?**
 - Forward-thinking DRAM vendors provide RC value on their web site
 - IBIS users need it

Proposal to Chip Vendors

- [PDN Model] is simple equivalent circuit
 - This keyword is just option
 - Standard format for On-Die PDN model
- [PDN Model] is essential for SI/PI Simulation like any other IBIS keywords
 - This keyword can help you and your customers
 - **Make the most of this keyword !**



```
[PDN Model] Decap
C_pdn
R_pdn
R_leak
[End PDN Model]
```

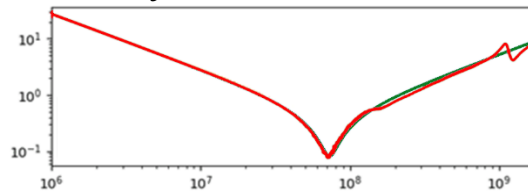
Only 9 values

Can keep secret ?

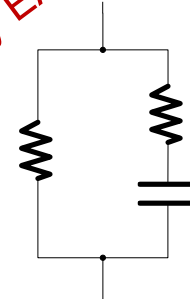
- Provide encrypted SPICE model



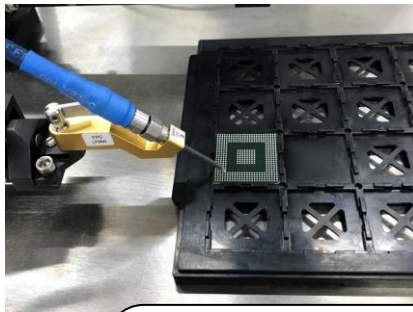
AC analysis



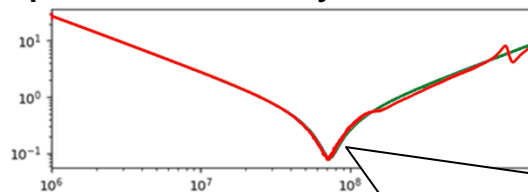
Very EASY



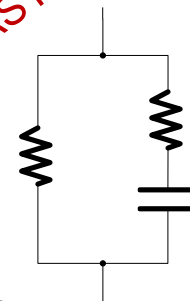
- Do not provide any models



Measurement by impedance analyzer



EASY



Measurement Trial by JEITA

Design value : 5.294nF

Measurement result : 5.422nF ~ 5.573nF (#22 chips)

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Conclusion

- Basics of On-Die PDN Model
 - Simple RC model
- Examples
 - Simulation results with and without On-Die PDN model are completely different
- Proposal to Chip Vendors
 - Make the most of this keyword !
- Thank you for your support on BIRD198.3 !

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