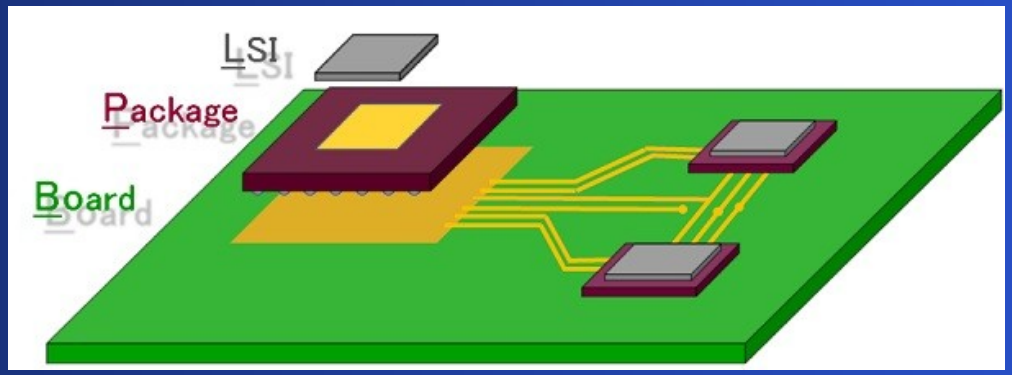
LSI Package Board needs…

- Mutual Communication
- Design Consistency
- Shorten Development Time

Enabled by

LPB format

New Standard



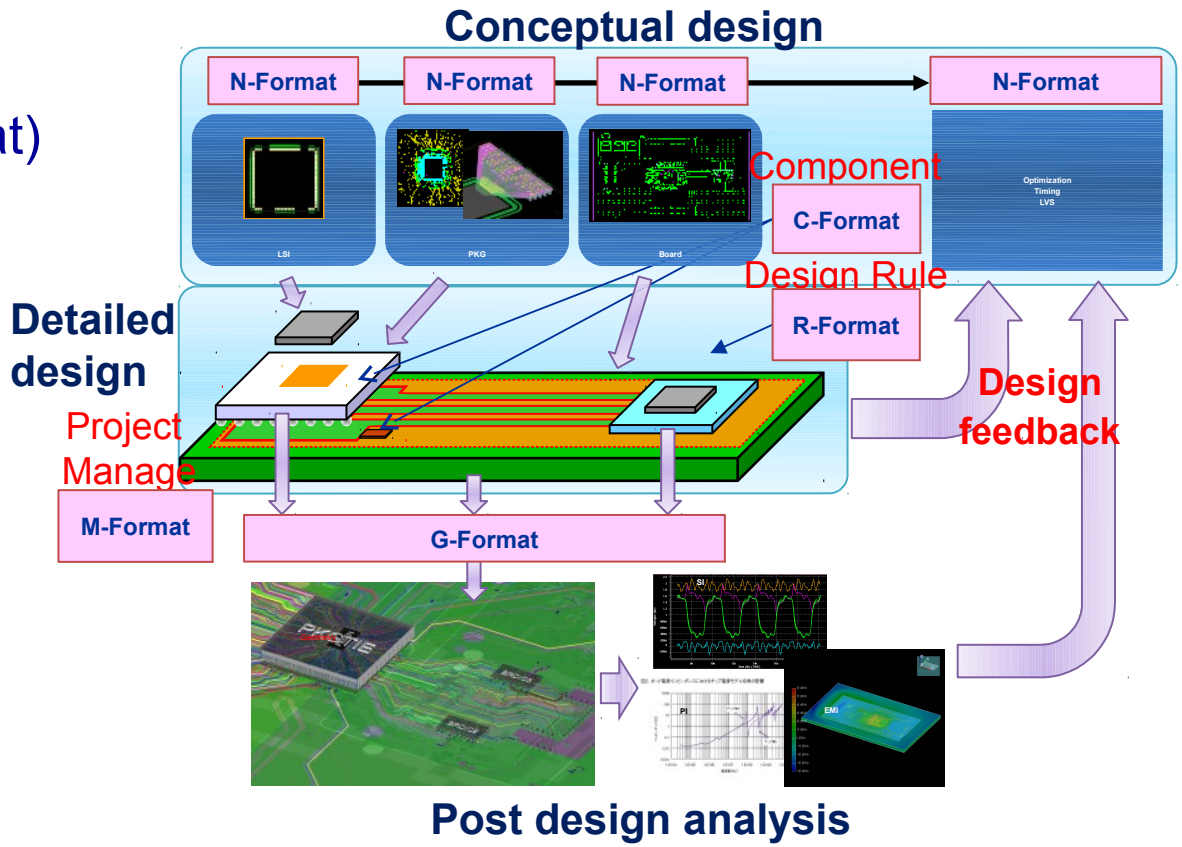
Agenda and Speakers

- EDA - example of design tool
  - Kazunari Koga　　Zuken
- EDA – example of modeling/simulations
  - Toru Watanabe　　ANSYS
- Summary : Benefits

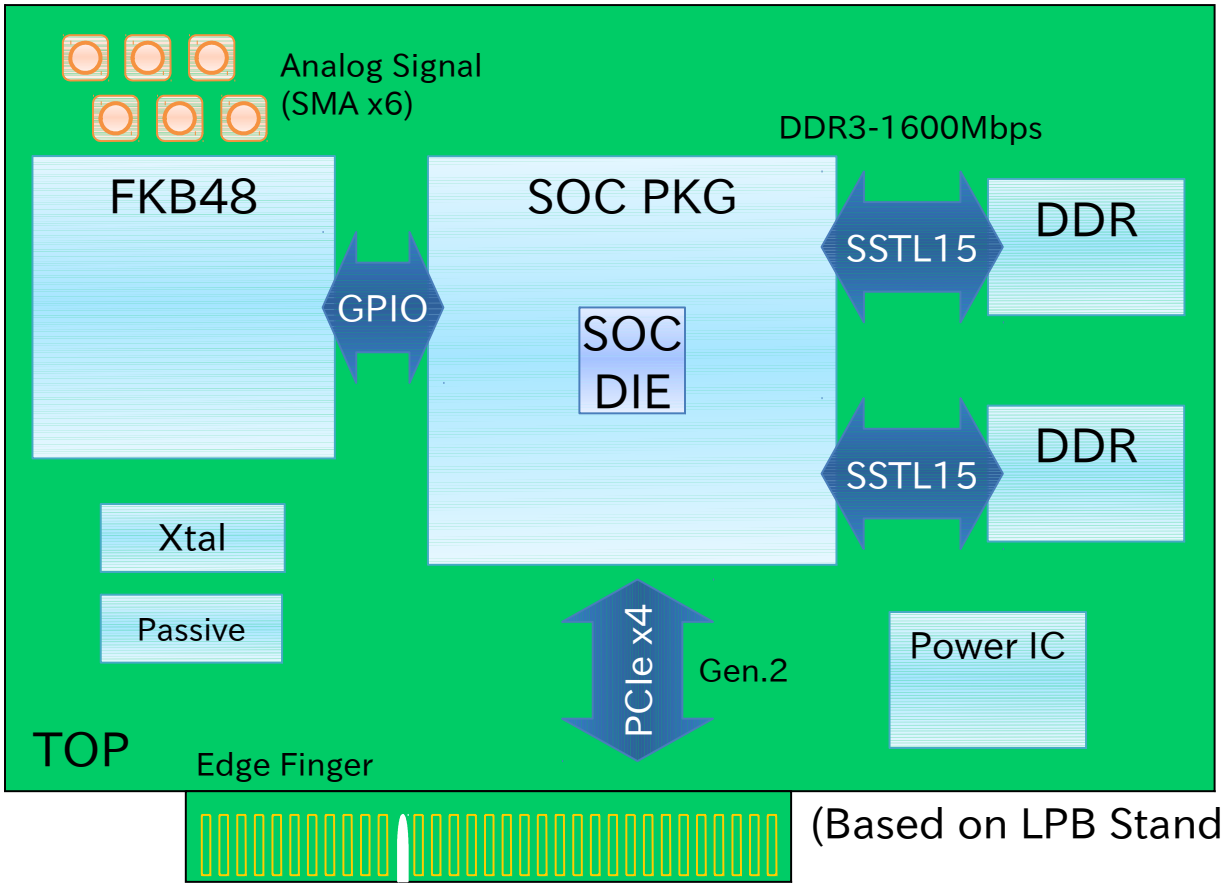
LPB Standard Format

Design environment to be constructed by 6 formats

1. Project Manage (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Design Rule (R-Format)
5. Geometry (G-Format)
6. Glossary



LPB sample files for test bench

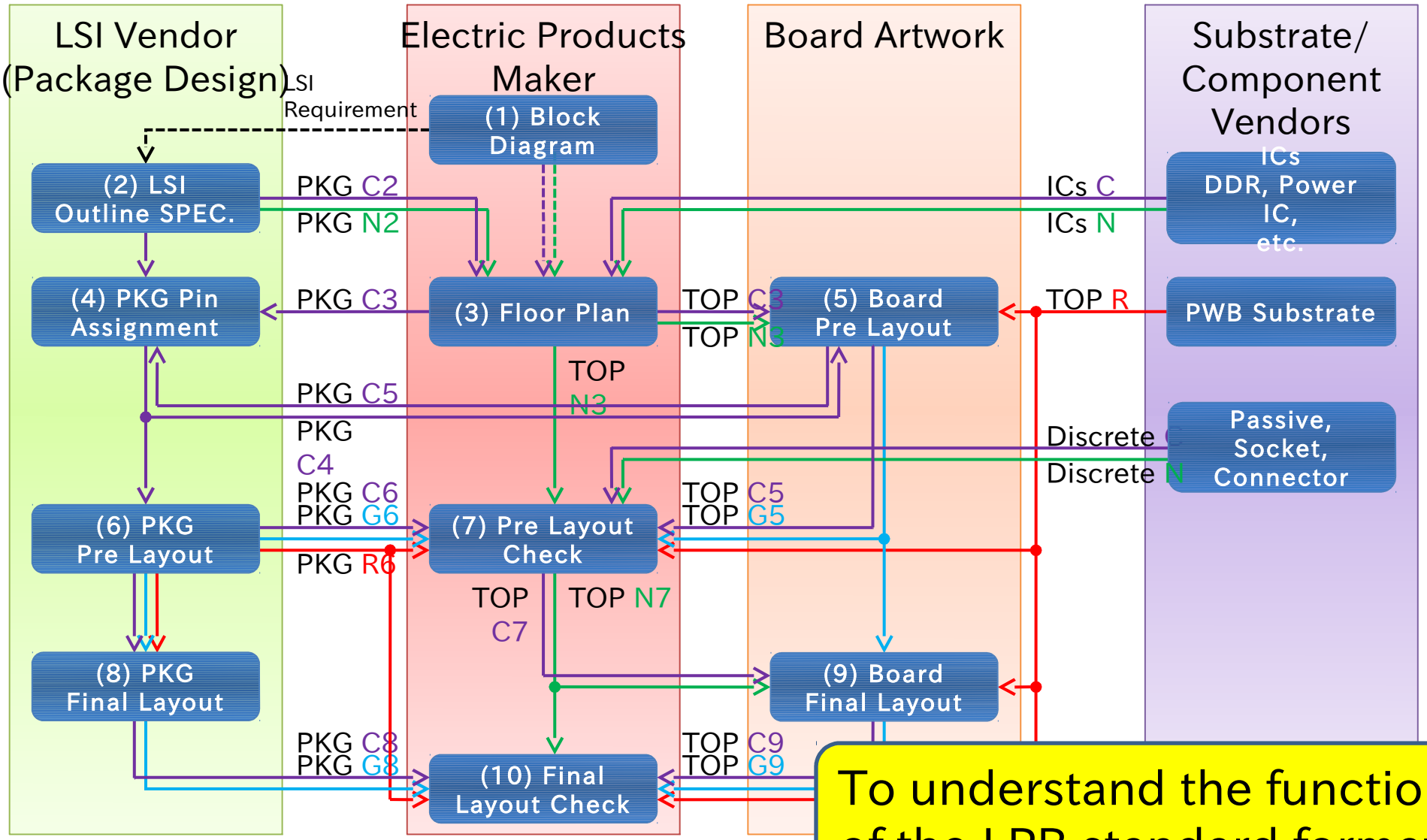


Component	Details
SOC	New Design
DDR	generic parts
FKB48	generic parts
Power IC	generic parts
Xtal	generic parts
Passive	generic parts

(Based on LPB Standard Format Ver.2.1)

Golden Sample are provided as a test bench for implementation.

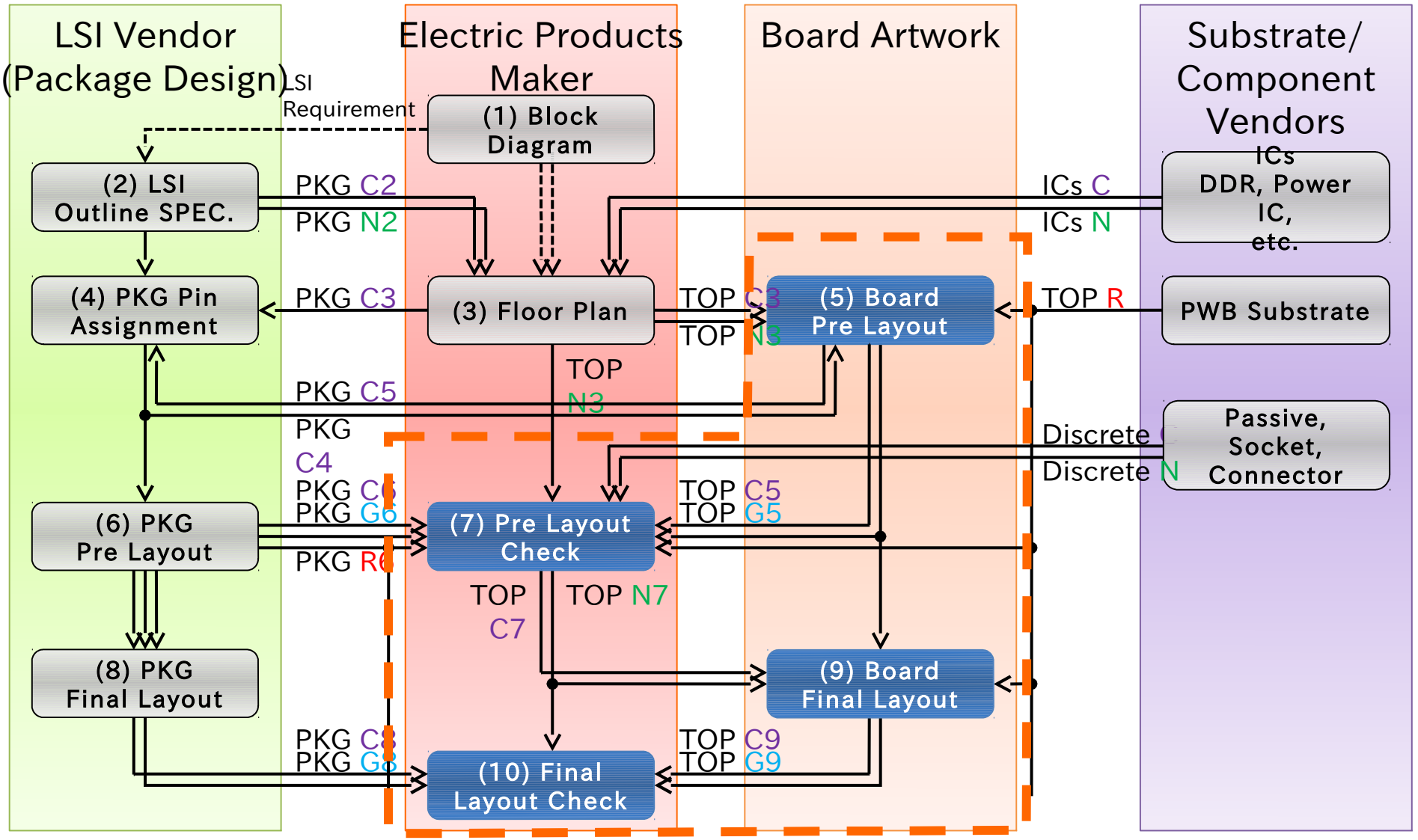
Reference flow using LPB standard format



To understand the function of the LPB standard format

Reference Flow Demonstration

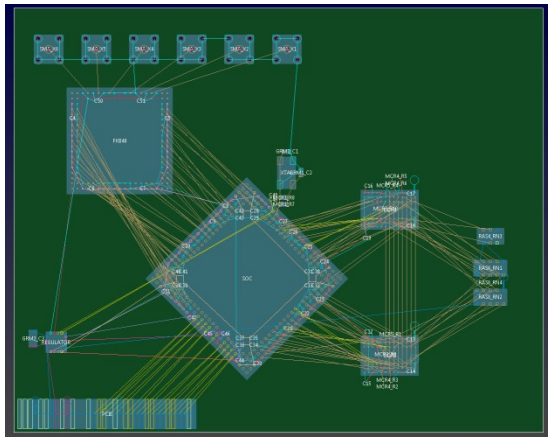
Reference flow using LPB standard format



(5) Board　Pre Layout

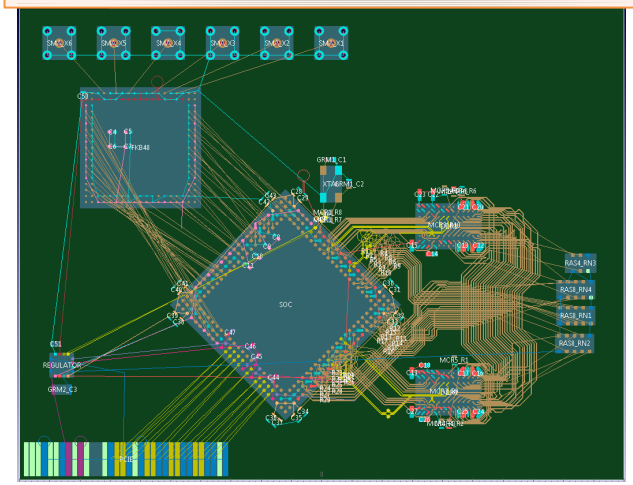
Design Force CR-8000

LPB format



Floorplan Result.
Tentative pin assignment is done.

Optimize Placement



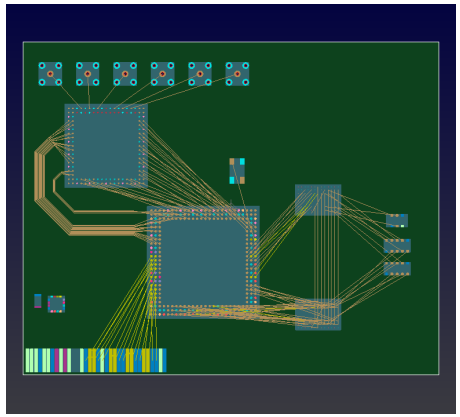
Critical Path Routing

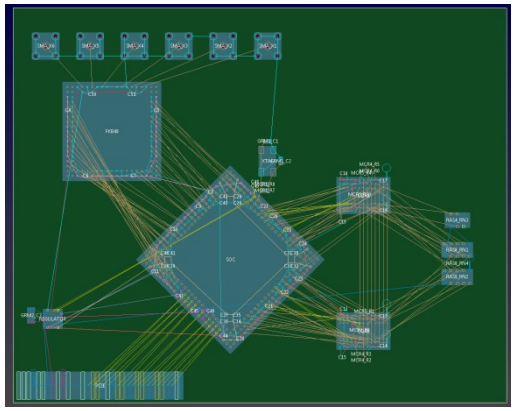
LPB format

Add the change of floorplan and pin assignment.

(5) Board　Pre Layout

Change placement info.





```
<placement y="-8223.2" x="30206.5" mount="TOP" angle="270" z="200" inst="DDR0"
ref_module="DDR"/> <placement y="15911.7" x="36947.6" mount="TOP" angle="270" z="200"
inst="DDR1" ref_module="DDR"/>
<placement y="-6500" x="400" mount="TOP" angle="0" z="200" inst="SOC"
ref_module="SOC_PKG"/>
<placement y="22417.2" x="-8150.9" mount="TOP" z="20" inst="GRM1_C1" ref_module="GRM1"/>
<placement y="23603.4" x="-4479.3" mount="TOP" z="20" inst="GRM1_C2" ref_module="GRM1"/>
```

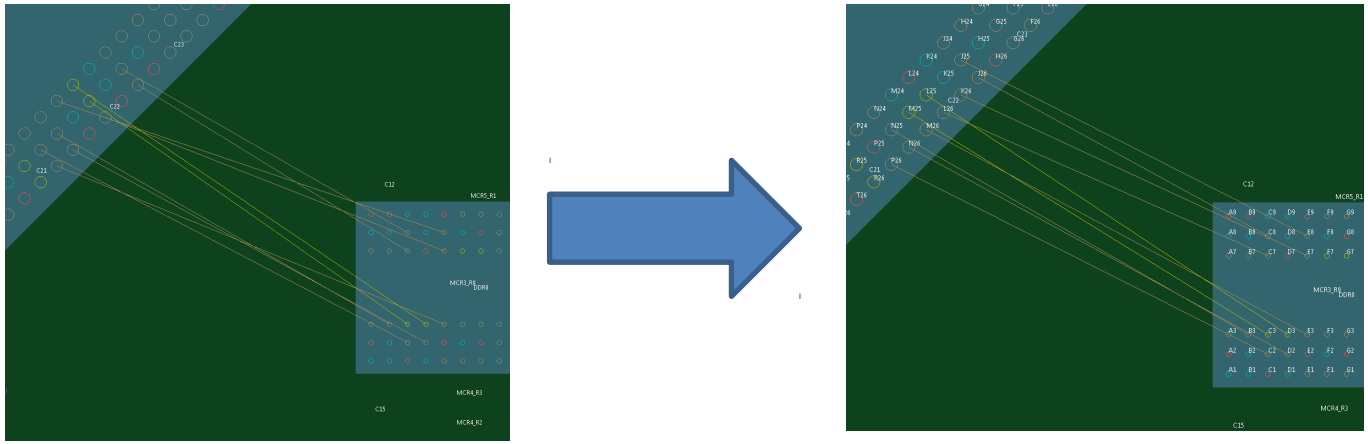
TOP C3

TOP C5

```
ref_module="DDR"/> <placement y="10911.7" x="30947.6" mount="TOP" angle="90" z="200"
inst="DDR1" ref_module="DDR"/>
<placement y="-6500" x="400" mount="TOP" angle="45" z="200" inst="SOC"
ref_module="SOC_PKG"/>
<placement y="22417.2" x="-8150.9" mount="BOTTOM" z="20" inst="GRM1_C1"
ref_module="GRM1"/>
<placement y="23603.4" x="-4479.3" mount=" BOTTOM " z="20" inst="GRM1_C2"
ref_module="GRM1"/>
```

(5) Board　Pre Layout

Swap pin



```
<port id="R24" type="signal" y="-1500" x="10500" name="DDRDQ[0]" direction="inout"/>
<port id="R25" type="signal" y="-1500" x="11500" name="DDRDQ[1]" direction="inout"/>
<port id="R26" type="signal" y="-1500" x="12500" name="DDRDQ[2]" direction="inout"/>
<port id="P24" type="signal" y="  -500" x="10500" name="DDRDQ[3]" direction="inout"/>
<port id="P25" type="signal" y="  -500" x="11500" name="DDRDQ[4]" direction="inout"/>
<port id="P26" type="signal" y="  -500" x="12500" name="DDRDQ[5]" direction="inout"/>
```

PKG C4

```
<port id="R24" type="signal" y="-1500" x="10500" name="DDRDQ[7]" direction="inout"/>
<port id="R25" type="signal" y="-1500" x="11500" name="DDRDQ[0]" direction="inout"/>
<port id="R26" type="signal" y="-1500" x="12500" name="DDRDQ[2]" direction="inout"/>
<port id="P24" type="signal" y="  -500" x="10500" name="DDRDQ[6]" direction="inout"/>
<port id="P25" type="signal" y="  -500" x="11500" name="DDRDQ[3]" direction="inout"/>
<port id="P26" type="signal" y="  -500" x="12500" name="DDRDQ[4]" direction="inout"/>
```

PKG C5

Simulation Setup

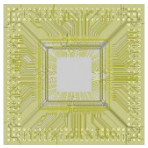
Input for Simulation:

Layout Tools :

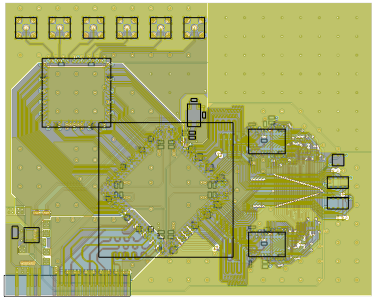
- Zuken　Design Force
- Cadence　APD
- etc…

- Board, Package Geometry
  - Traces, Vias, Pads
  - Planes, Polygons
  - etc…

G-Format



Package
Designed by APD



Board
Designed by Design Force

Extraction Tools :

- ANSYS　ANSYS SIwave, ANSYS HFSS
- etc…

Simulation Setup

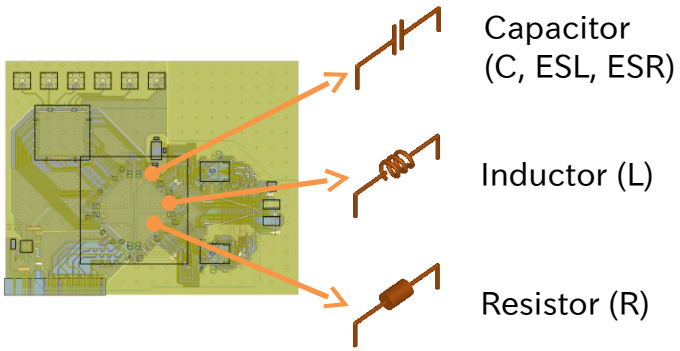
Input for Simulation:

Layout Tools :

- Zuken　Design Force
- Cadence　APD
- etc…

- Passive Components
  - C, L, R
- Constraints
  - Skew, Frequency, etc…

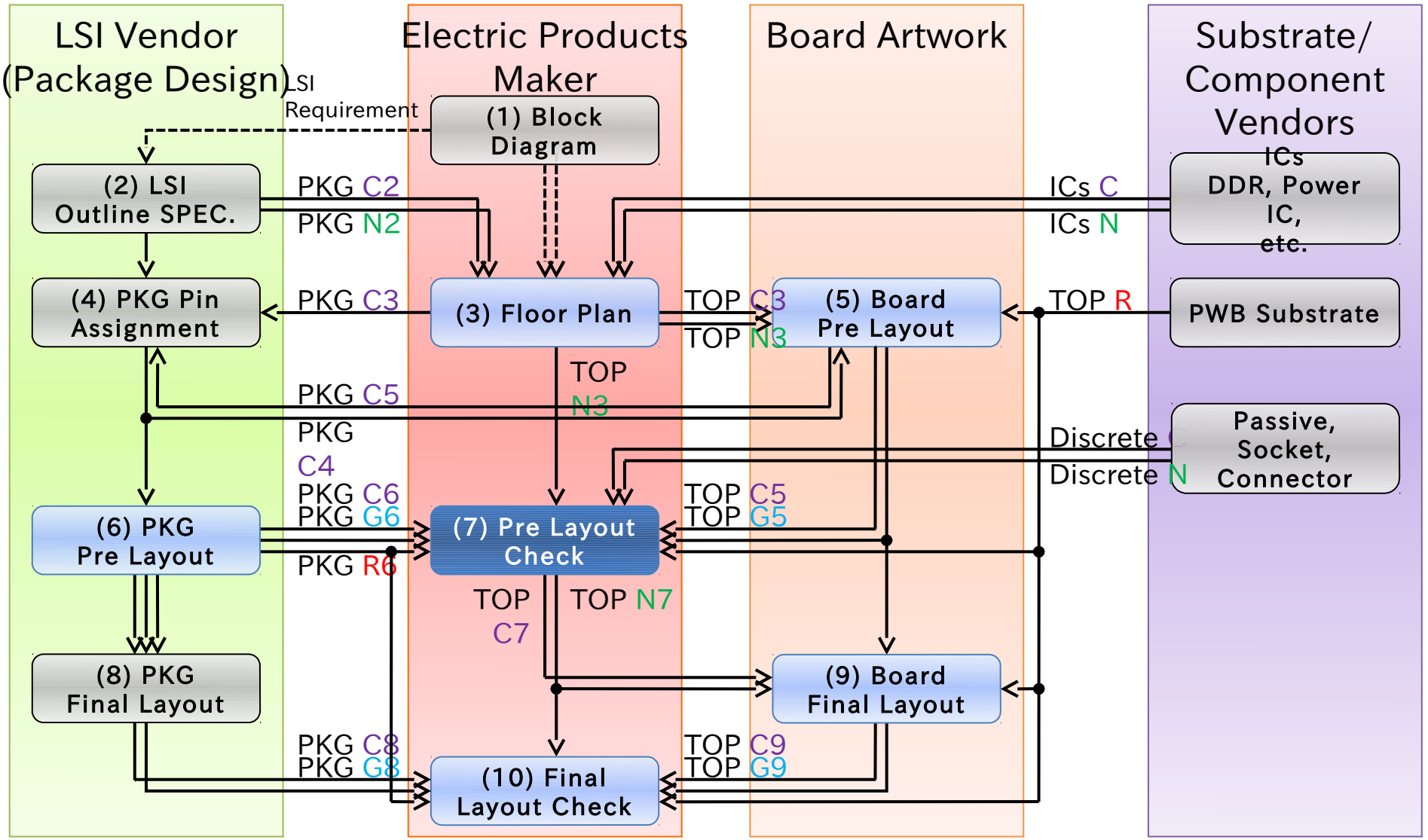
C-Format



Extraction Tools :

- ANSYS　ANSYS SIwave, ANSYS HFSS
- etc…

(7) Pre Layout Check



(7) Pre Layout Check

Works：

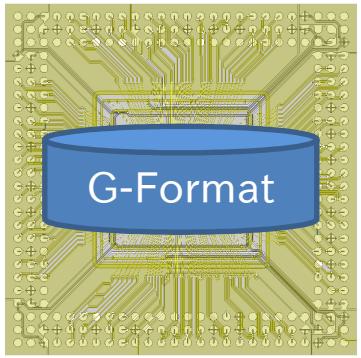
(7) Pre Layout Check

- 【Signal Integrity Simulation of Critical Nets】
- Timing Verification of DDRIII 1.3GBps Write Cycle
  - Is Damping Resistors required?
  - What is the best ODT setting?
  - Estimate the worst skew of DQ

(7) Pre Layout Check

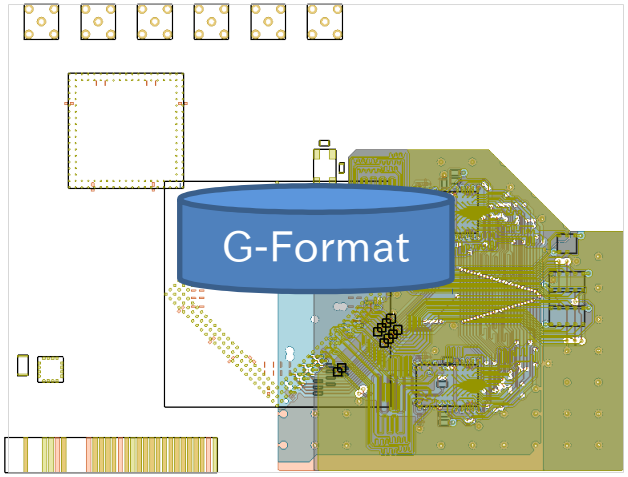
Geometry :

【Package】



- Designed by Cadence APD
- All nets are completely routed
- DQs are NOT isometric

【Board】



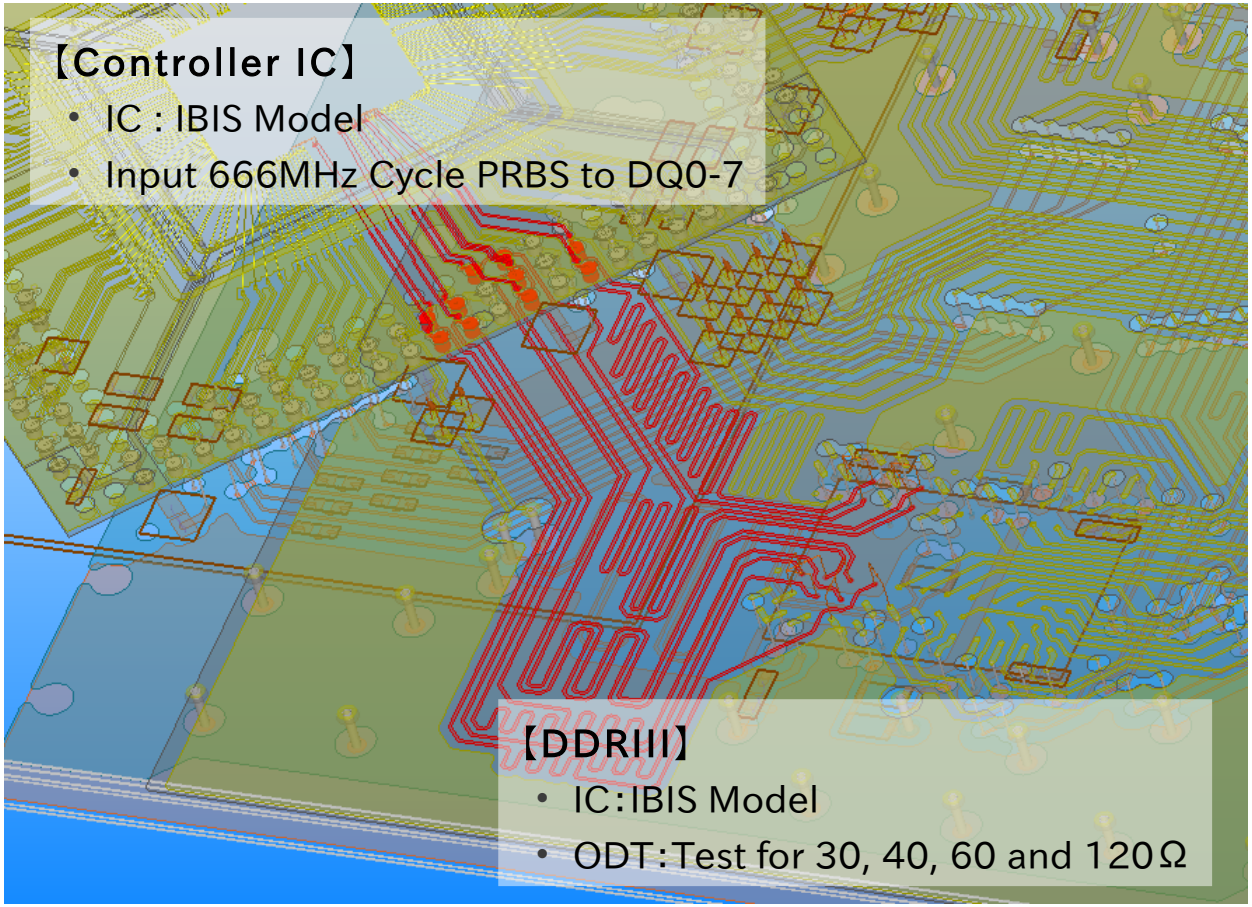
- Designed by Zuken Design Force
- Only 1.5V Power, Ground, DQS and DQ
- DQS and DQs are isometric

ANSYS SIwave

Merged and stacked in Extraction Tool

(7) Pre Layout Check

Overview of Simulation :



DQS, DQ signals in Package and Board Layout / ANSYS SIwave (Extraction Tool)

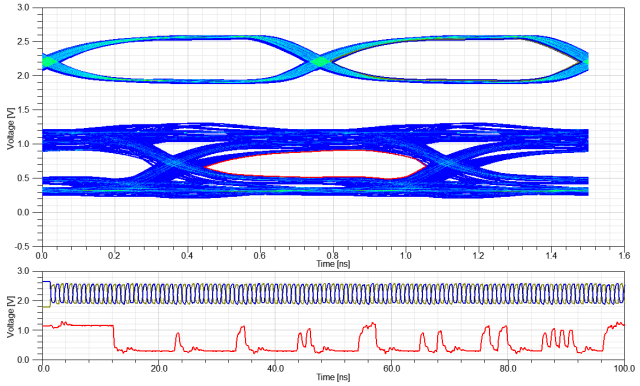
(7) Pre Layout Check

Simulation Result :

Eye Diagram (ODT:30Ω (FAIL))

DQS

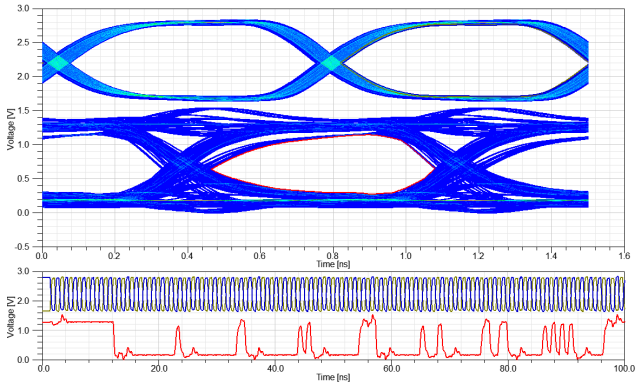
DQ0



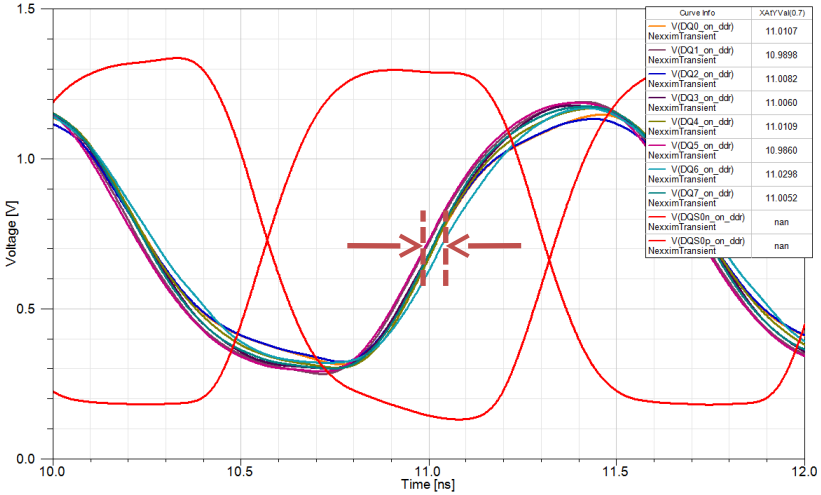
Eye Diagram (ODT:60Ω (Best Case))

DQS

DQ0



Transient Waveform of DQS and DQ0～7



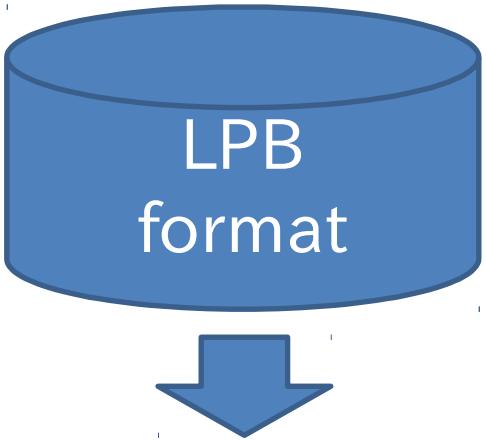
【Worst Skew (Case of ODT=60Ω)】

- 42.8ps (DQ5-DQ6)

Eye Diagram and Transient Waveform / ANSYS DesignerSI (Circuit Simulator)

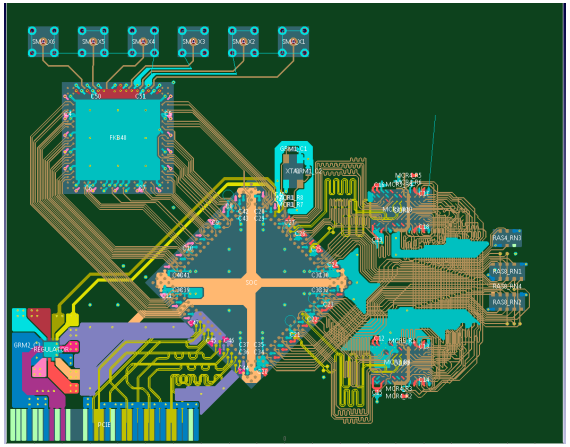
(9) Board　Final Layout

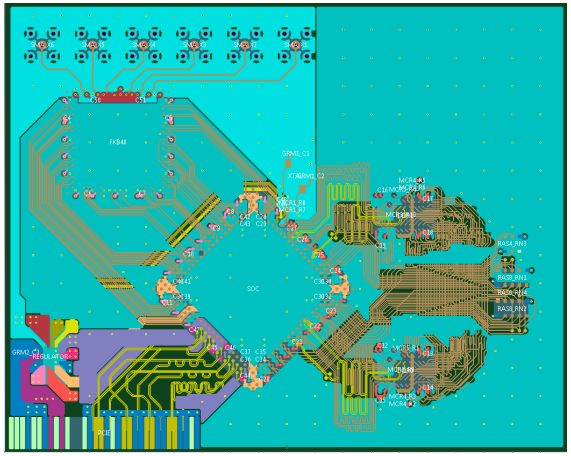
Import the result of pre layout check
- Skew
- Decap



Re design to satisfy the constraints.
- Change pin assignment
- Change decap

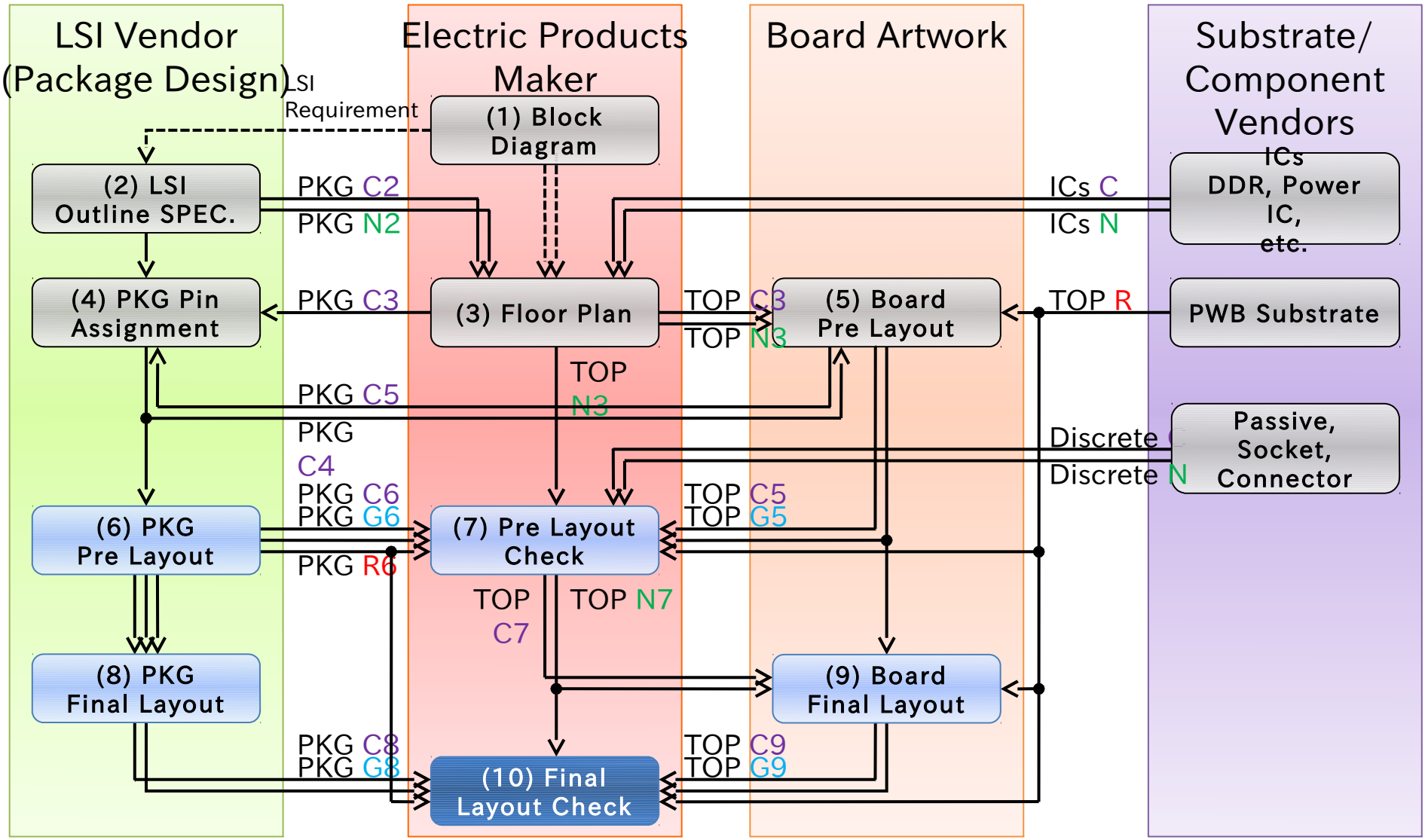
Route other signal
Design power/ground





Design Force
CR-8000

(10) Final Layout Check



(10) Final Layout Check

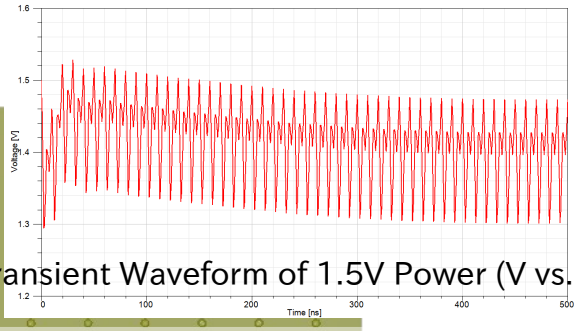
Works：

(10) Final Layout Check

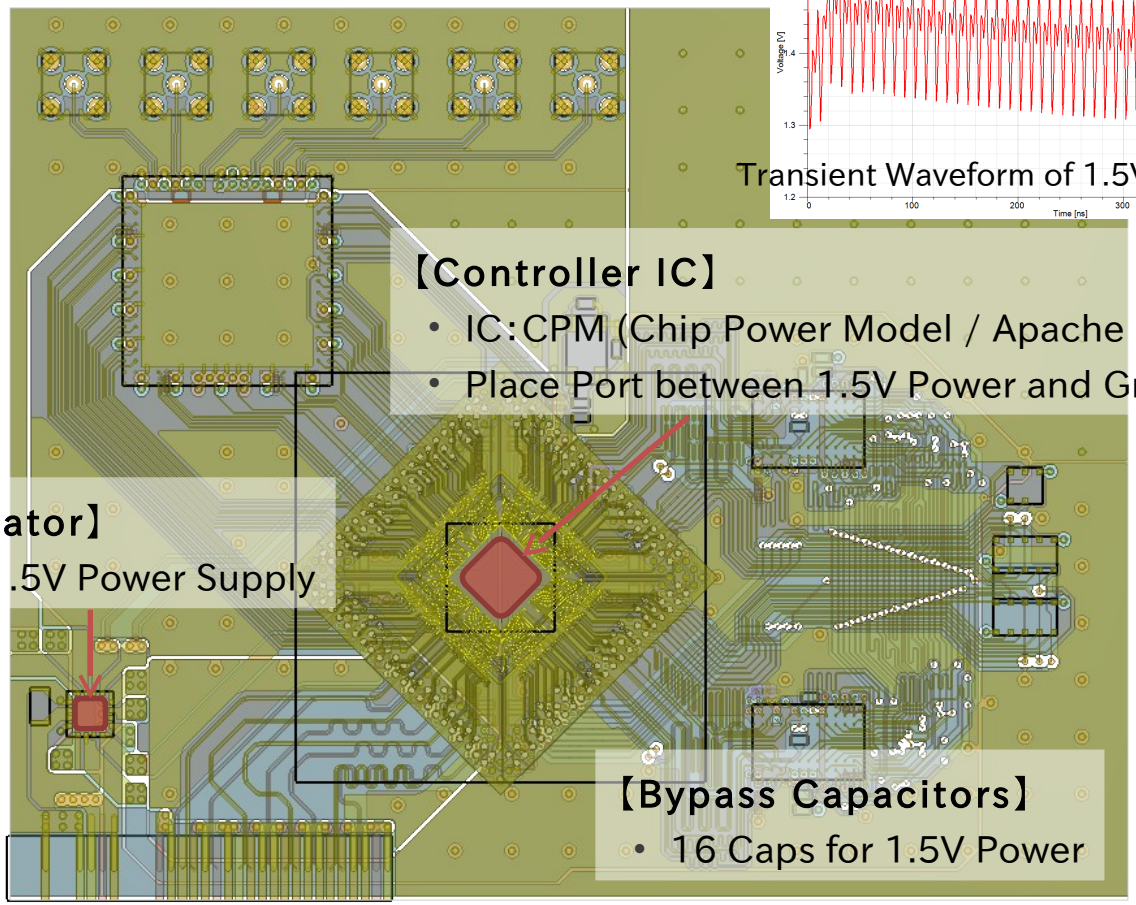
- 【Power Integrity Simulation of PDN】
- Input Impedance Analysis of Controller IC and Bypass Caps Optimization
  - Chip-Package-System Total Impedance
  - Bypass Caps Optimization
- 【EMI (Far/Near Field) Simulation】
- Far/Near Field analysis induced by Power Noise
  - CISPR 22 Test (Far Field)
  - Checks Near Field

(10) Final Layout Check

Overview of Simulation :



Transient Waveform of 1.5V Power (V vs. T)



【Controller IC】
- IC：CPM (Chip Power Model / Apache RedHawk)
- Place Port between 1.5V Power and Ground

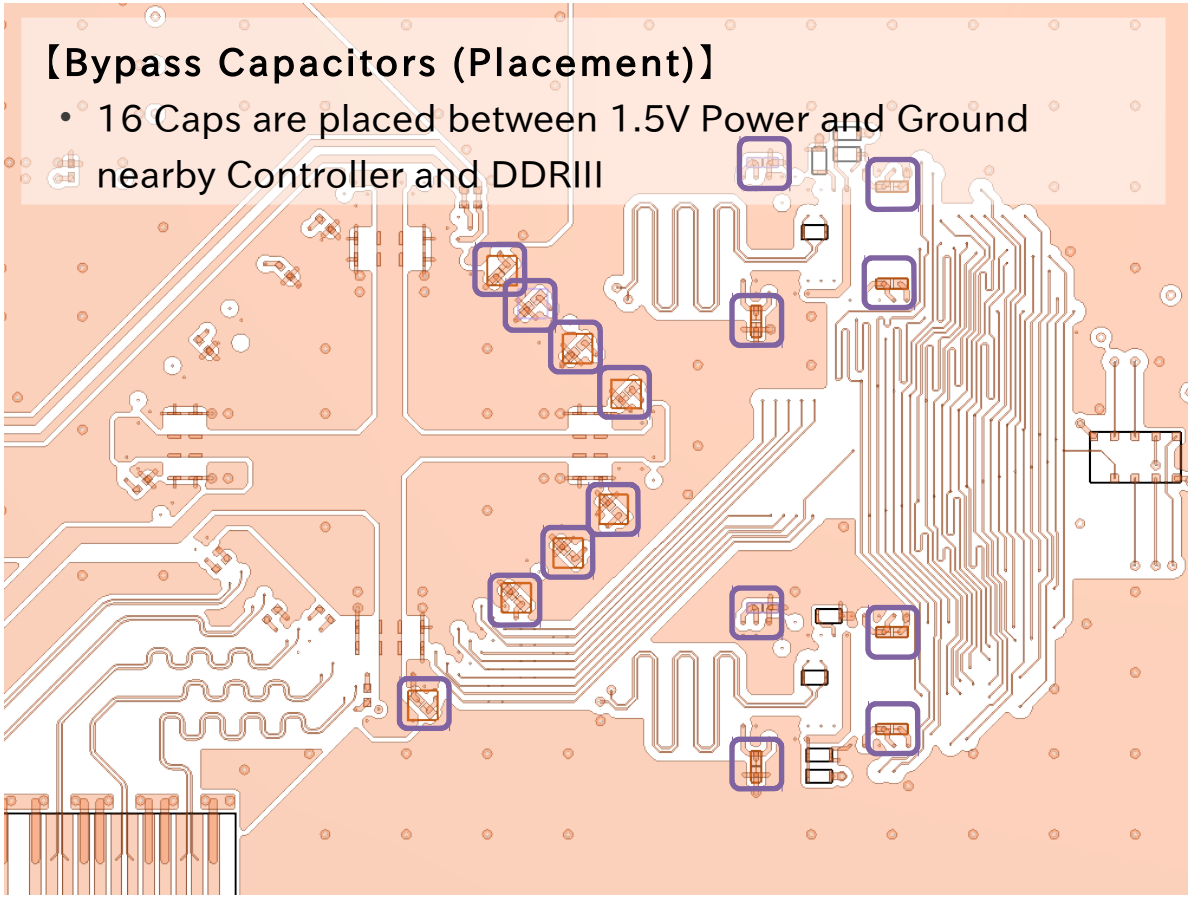
【Regulator】
- DC 1.5V Power Supply

【Bypass Capacitors】
- 16 Caps for 1.5V Power

Package and Board Layout / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

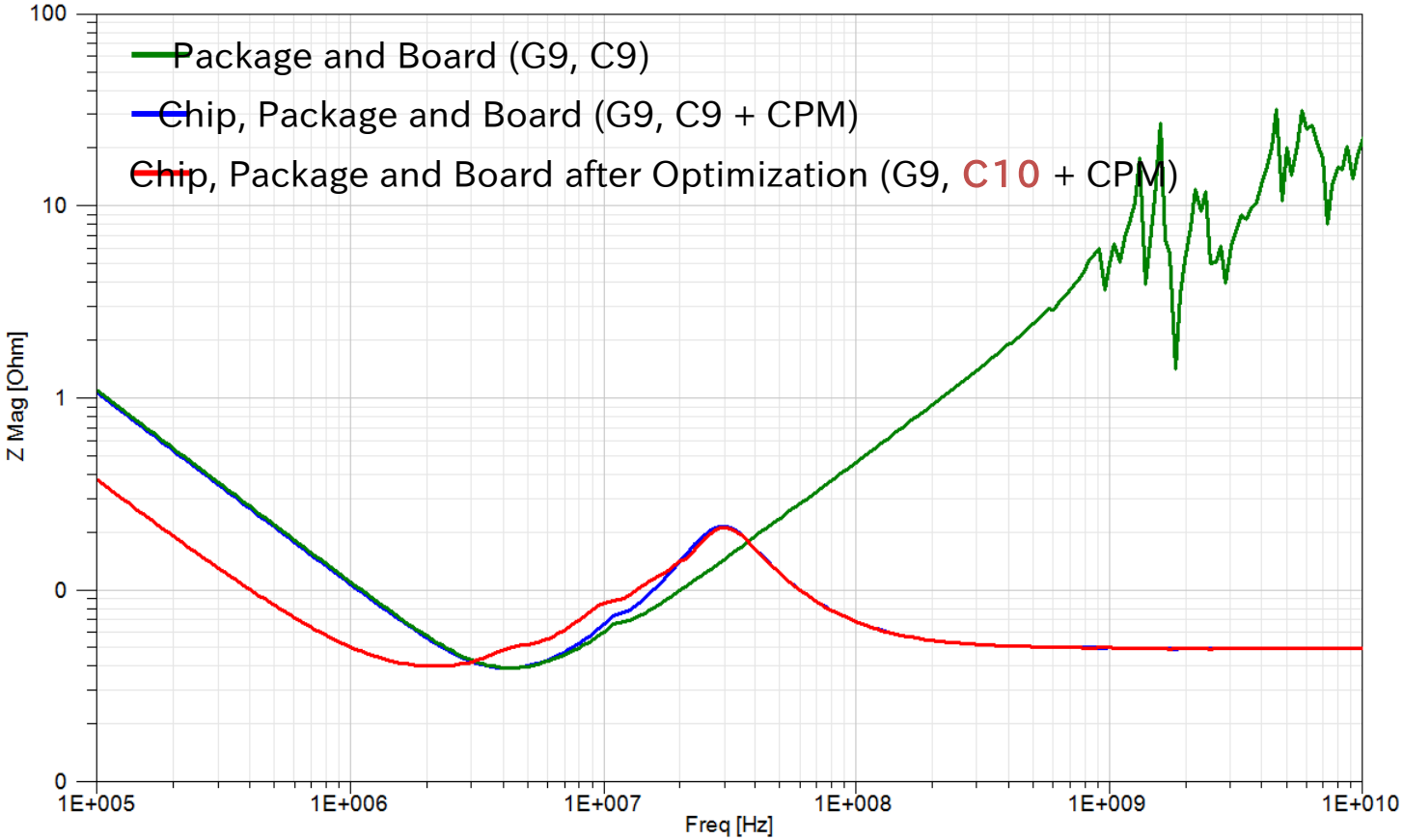
Overview of Simulation :



Bypass Caps Placement (Bottom Layer) / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

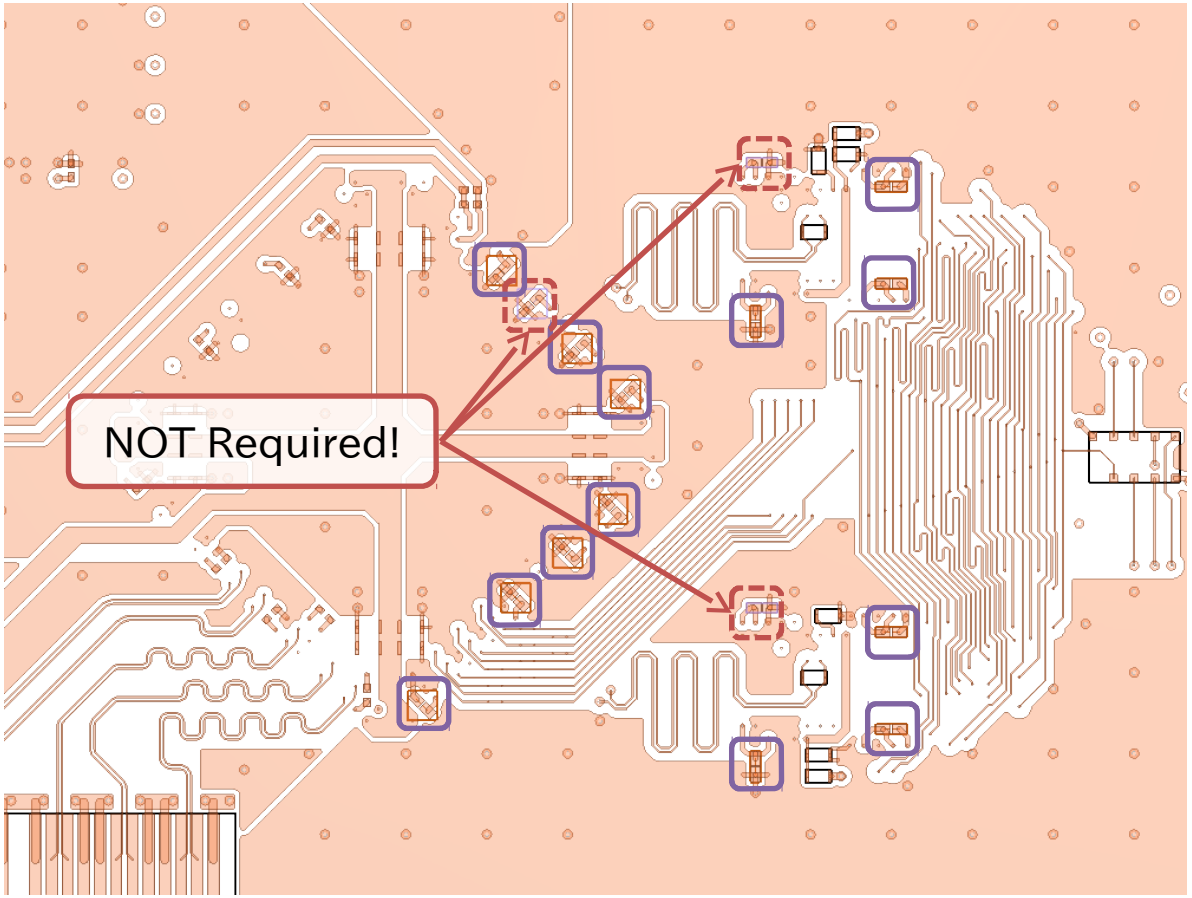
Simulation Result :



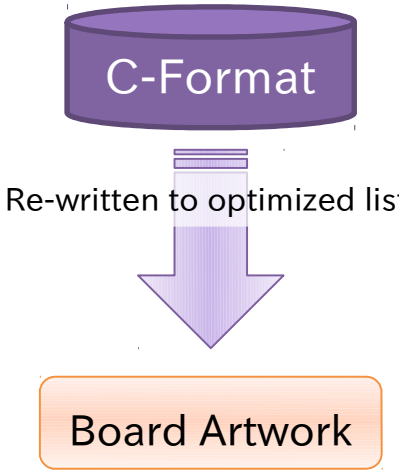
Input Impedance of 1.5V Power on Controller IC / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

Simulation Result :



Bypass Caps Placement (Bottom Layer) / ANSYS SIwave (Extraction Tool)

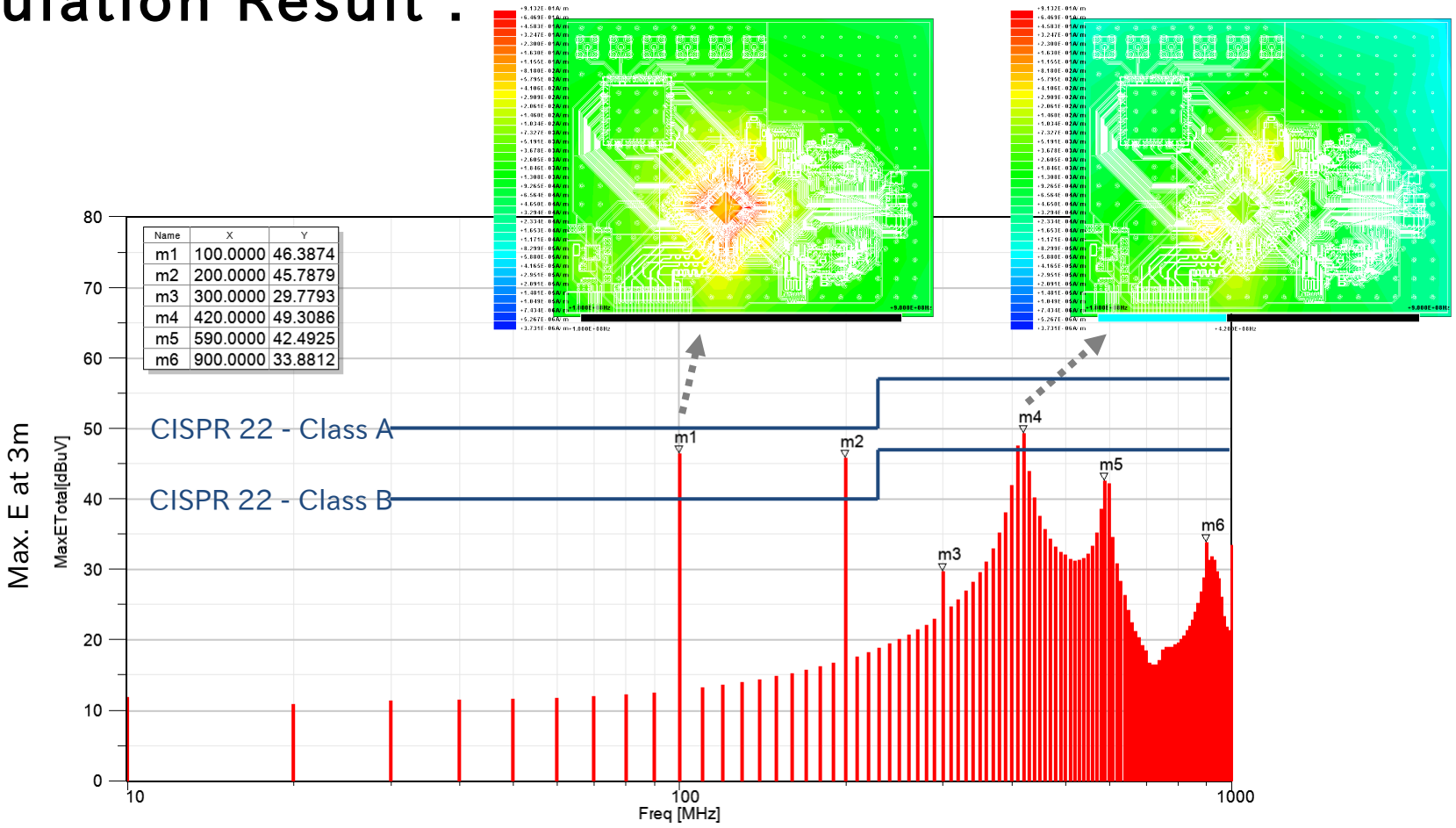


(10) Final Layout Check

Simulation Result :

H-field 1mm above (100MHz)

H-field 1mm above (420MHz)



Far Field and Near Field / ANSYS SIwave (Extraction Tool)

(10) Final Layout Check

Works：

(10) Final Layout Check

- 【Power Integrity Simulation of PDN】
- Input Impedance Analysis of Controller IC and Bypass Caps Optimization
  - Chip-Package-System Total Impedance ⇒ **OK**
  - Bypass Caps Optimization ⇒ **Optimized**
- 【EMI (Far/Near Field) Simulation】
- Far/Near Field analysis induced by Power Noise
  - CISPR 22 Test (Far Field) ⇒ **OK**
  - Checks Near Field ⇒ **OK**

Benefit of LPB format

- **Quick & Accurate design/simulation set up**
  - Enable EMC check from development early stage
  - No more e-mail/phone call/meetings
  - Avoid human error; eliminate hand edit, version control
- **Feedback can be done from any parties, and instantly.**
  - For optimization/cost down/quality up feed back
- **Easy implementation**
  - Human readable, open format XML/Verilog-HDL
  - XML parser available.
  - Simple / light geometry format (G-format:XFL)