Allegro X AI – Generative Design for PCB and Packaging

日本語訳版

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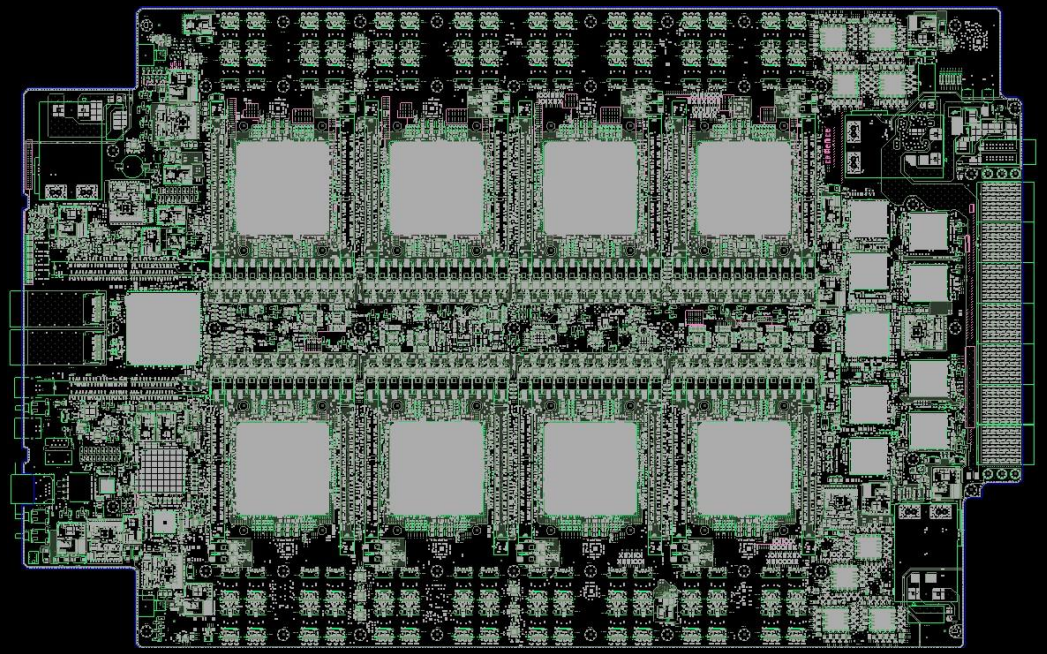
Recent State-of-the-Art PCB Designed with Allegro Platform



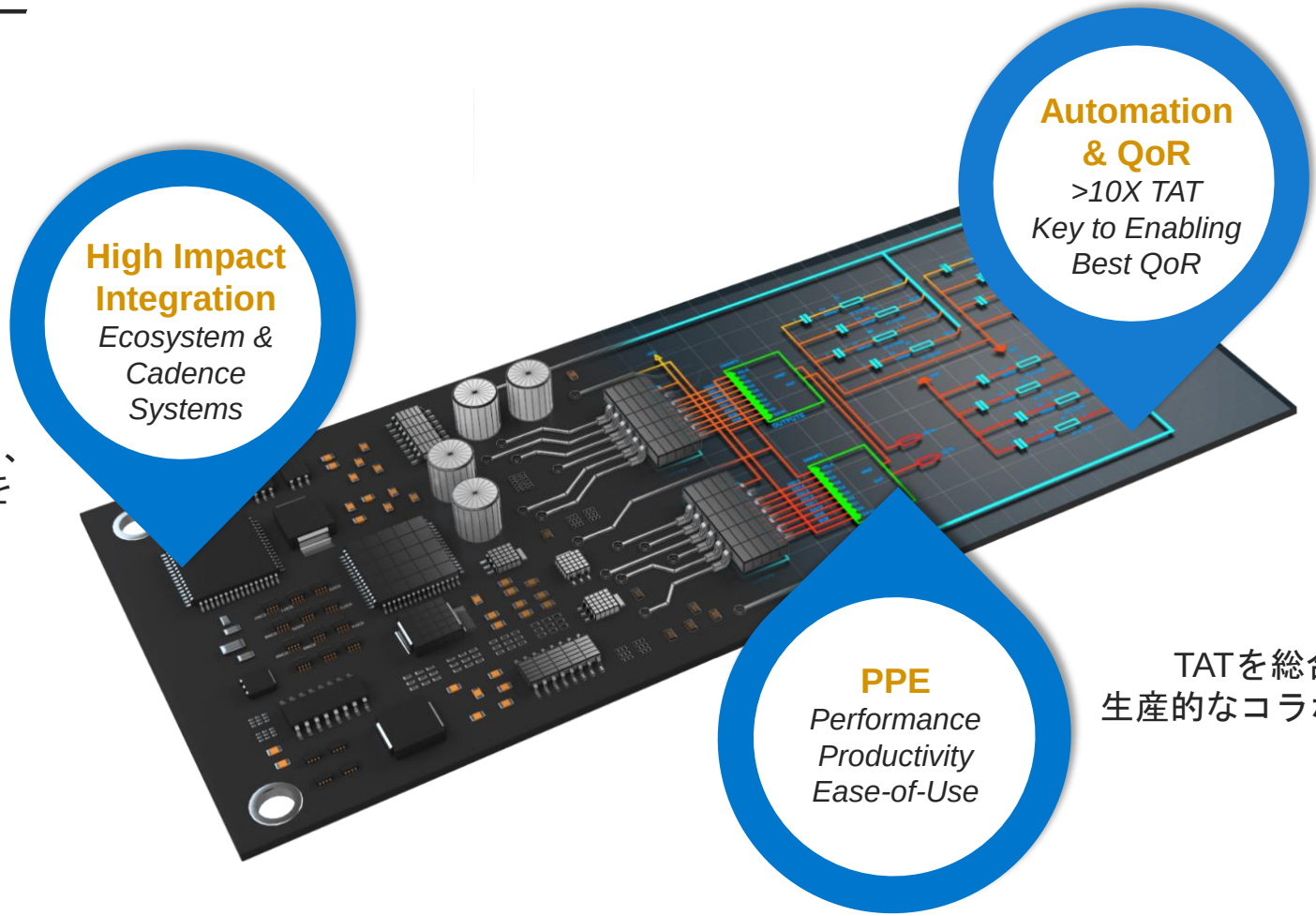
- Cadence® Palladium® Z2 Emulation Board
- 24” x 16” board size, 36 layers construction
- 20k+ components, 14k+ Nets, 25k+ Vias
- State-of-the-art materials: Megtron-6 di-electric and ultra-low-profile copper

What we learn through our customers fuels our vision and roadmap

Our Focus: Fastest TAT & Best Quality of Results(QoR)

3つのストラテジー

Cadence及びパートナーのソリューションを連携活用し、手戻りを削減して市場投入を飛躍的に加速させる



自動化によりTime To Marketのボトルネックを解消しゲームチェンジを図る

TATを総合的に削減し、生産的なコラボレーションを実現

Turnaround Time (TAT)

System & Mechanical | Schematic | Layout | Analysis | Manufacturing

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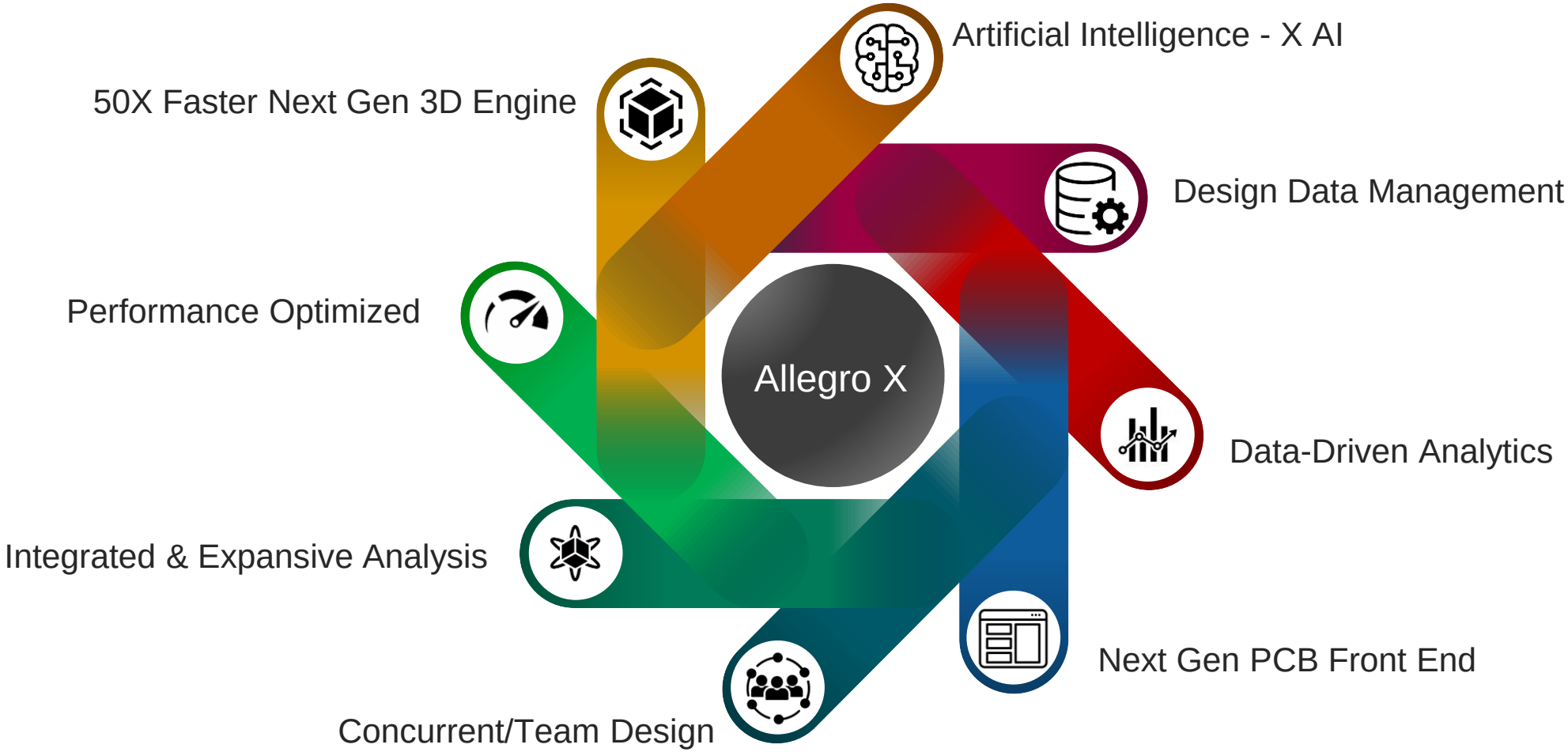
Allegro Xとは

Fastest TAT & Best QoR を可能にするCadenceの次世代PCBデザインプラットフォーム



AI/MLを利用した機能の開発状況

cadence.comで公開されたニュースリリース / ブログより

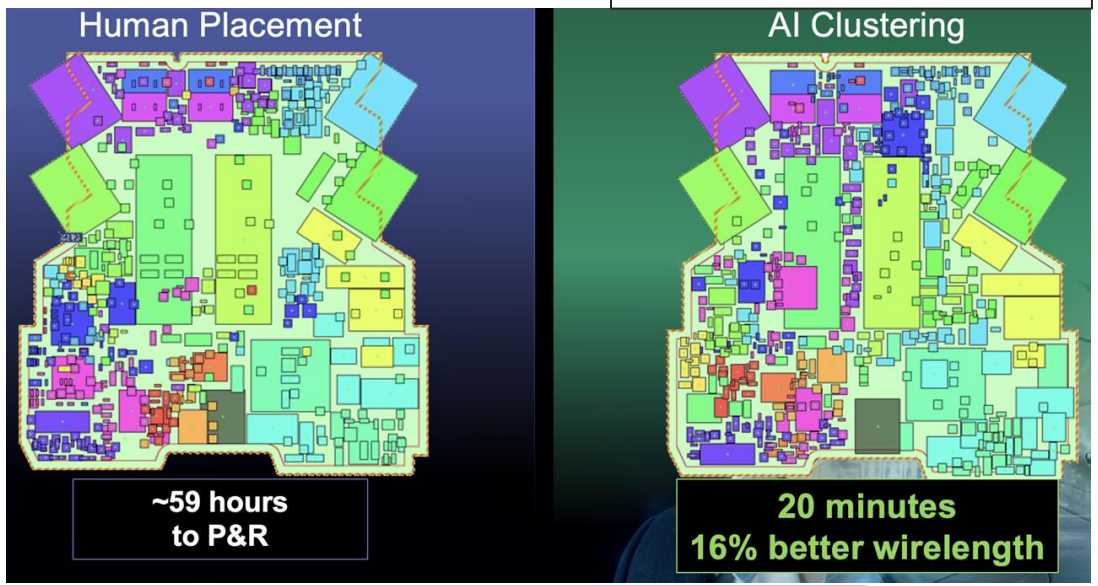
= ニュースリリース =

- ケイデンス、Allegro X AIを発表、TATを1/10以下に削減しPCB設計を加速

= ブログ =

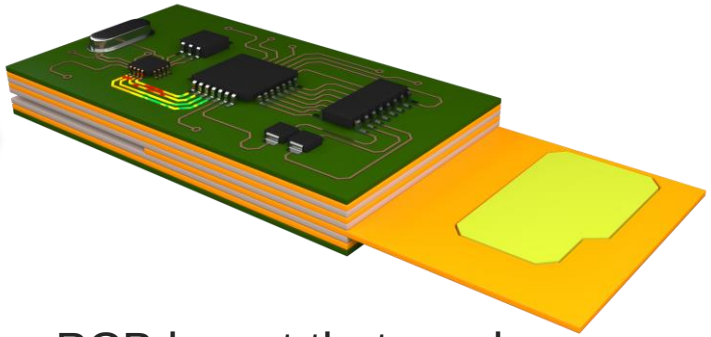
- Allegro X AIを含むAI開発状況について
  - DesignCon : Ben Guの基調講演から ～AI ソリューションの最前線 ～
- 解析での最適化にAIを活用する ‘Optimality’ に関する記事
  - Cadence Optimality AI により最大の問題(=人手の作業)を解決
  - AI/MLの活用により、分野の垣根を超えた解析と最適化を新たな生産性レベルにまで高める
  - Optimality Intelligent System Explorer

人手による配置 vs. AIによる配置



Allegro X AI のインプットとアウトプット
ICデジタル設計における自動化のアプローチをPCBにも適用

Design Netlist
and Constraints



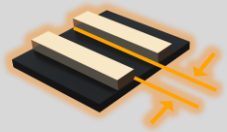
PCB layout that can be used as generated or incrementally modified

Allegro X AI メソドロジー – より詳細な情報として

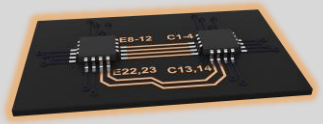
事前の制約定義により自動化 / ワークフローのシフトレフト / 結果の品質の向上が可能に

Layer Stack

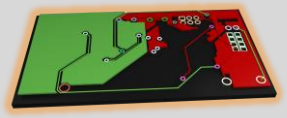
Board Outline - MCAD + fixed component location(s)



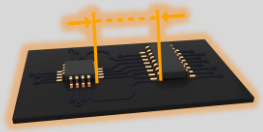
Physical constraints



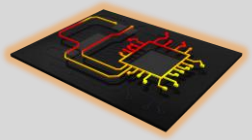
Netlist



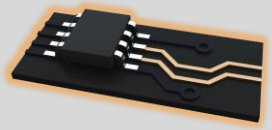
PWR/GND



Assembly rules

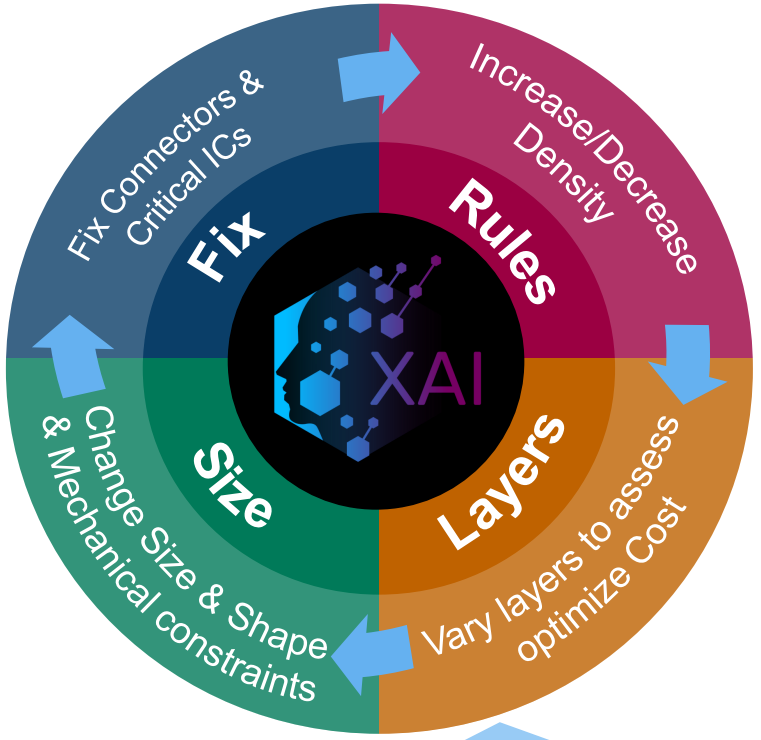


Power Distribution Network



Differential Pairs & Critical nets

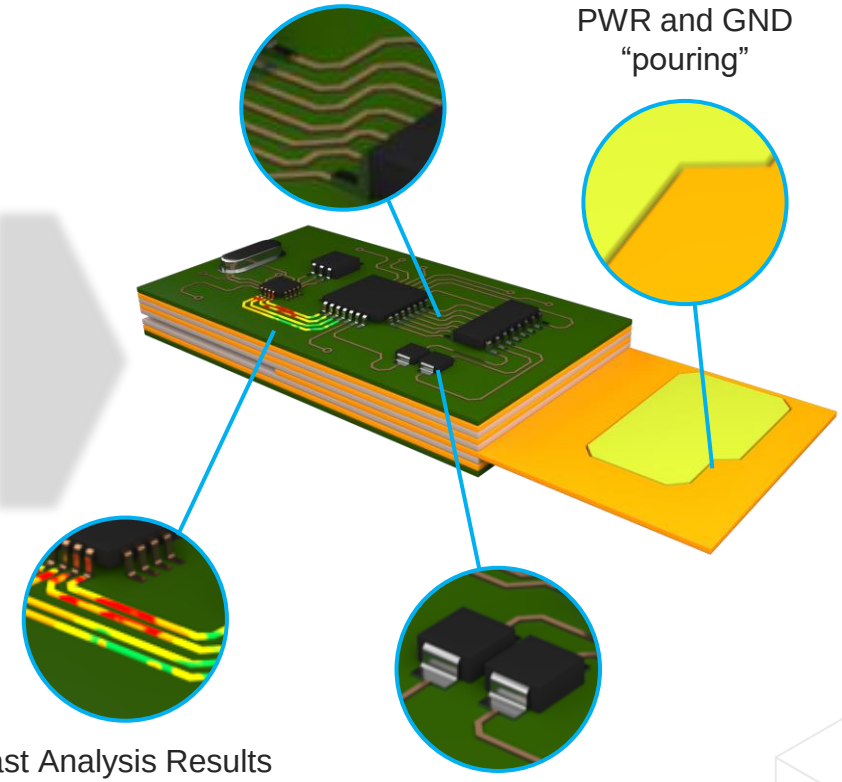
ソリューションスペースを迅速に探索



- **On CLOUD (AWS)**
- **Cadence educates the AI**
- **Never learn from customer's design**

Critical Routing (Now)
Full routing (2024)

PWR and GND "pouring"

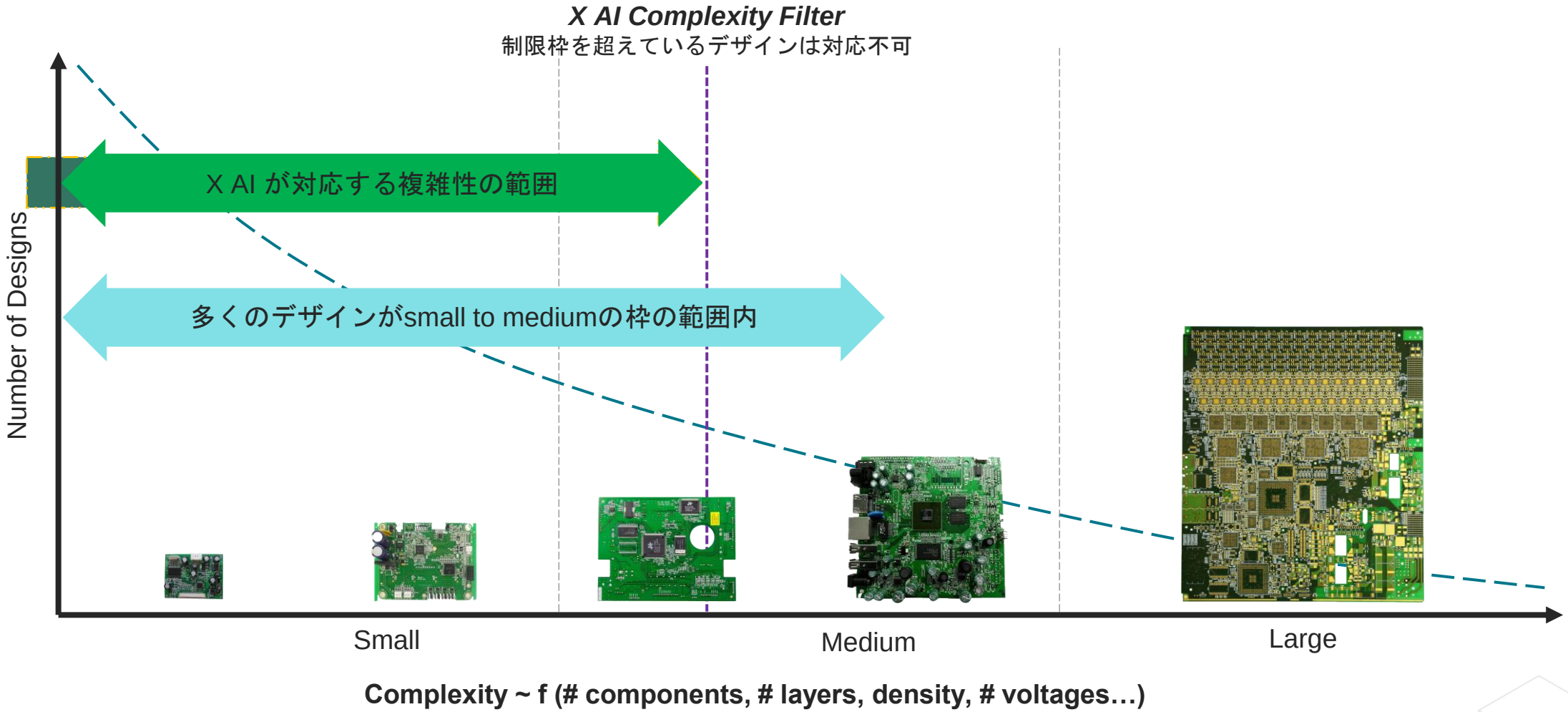


Fast Analysis Results (SI PI)

Board Placement

Allegro X AIのターゲットデザイン

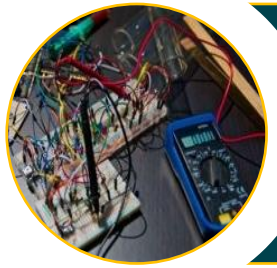
まずは低～中規模の複雑性のデザインから



Allegro X AI のステークホルダー毎の価値

Engineering Manager

- PCB開発チームからのアプトプットを増やし、効率向上
- デザインTATを短縮



Electrical Engineer

- PCBレイアウトへの貢献度を拡張
- 異なる条件でのレイアウトの試行 - デザインスペースの探索

PCB Designer

- X AI はPCB Designerの代わりになるものではなく、PCB Designerの新たなツールの一つ
- より多くの時間を複雑なPCBの課題にフォーカスできるようにし、生産性を向上
- PCBの洞察機会や新アイデアの創造機会を生み出し、最適化の可能性を拡大

Allegro X AI is Offered on Cadence AWS Cloud

Cloud servers and data security

- Powered by 1000s of scalable compute resources
- Provides AWS servers in USA
  - As usage scales additional server locations being considered
- Is not shared with any other Cadence cloud-based service
- Is ISO 27001 compliant
- Data can ONLY be accessed by customer
- No persistent training of AI engine with customer data
- Regular third-party penetration tests performed
- Design and corresponding data is deleted after session end
- Leverages all AWS Data Protection Services

Allegro X AI – What's Next?

- Currently Allegro® X AI is in controlled production availability
  - We are partnering with a limited number of early customers
    - Learning through early engagement
    - Improving "out-of-the-box" performance
    - Identifying ways to ease adoption and the associated use model paradigm shift
- We plan to broaden Allegro® X AI availability in Q4 2023
- Thank you for your time

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AI活用による解析～パラメータ最適化

Optimality

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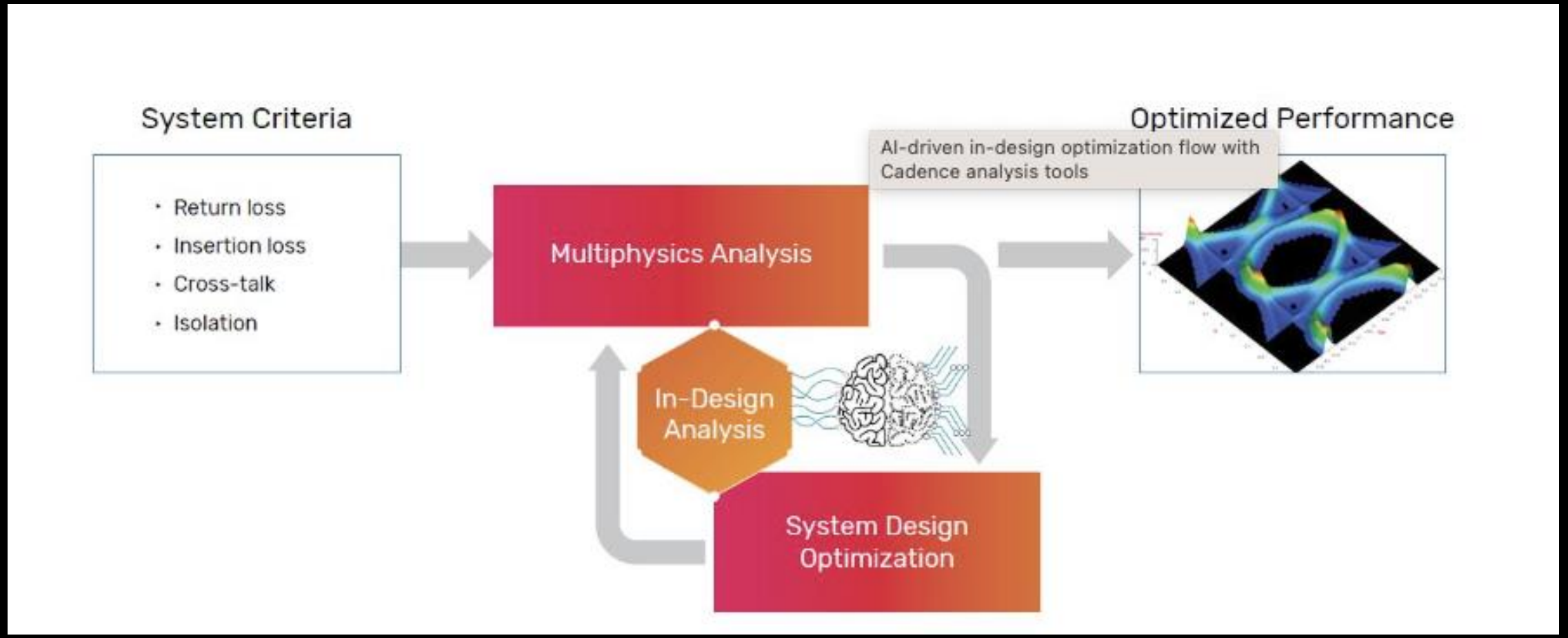
Optimality Intelligent System Explorer

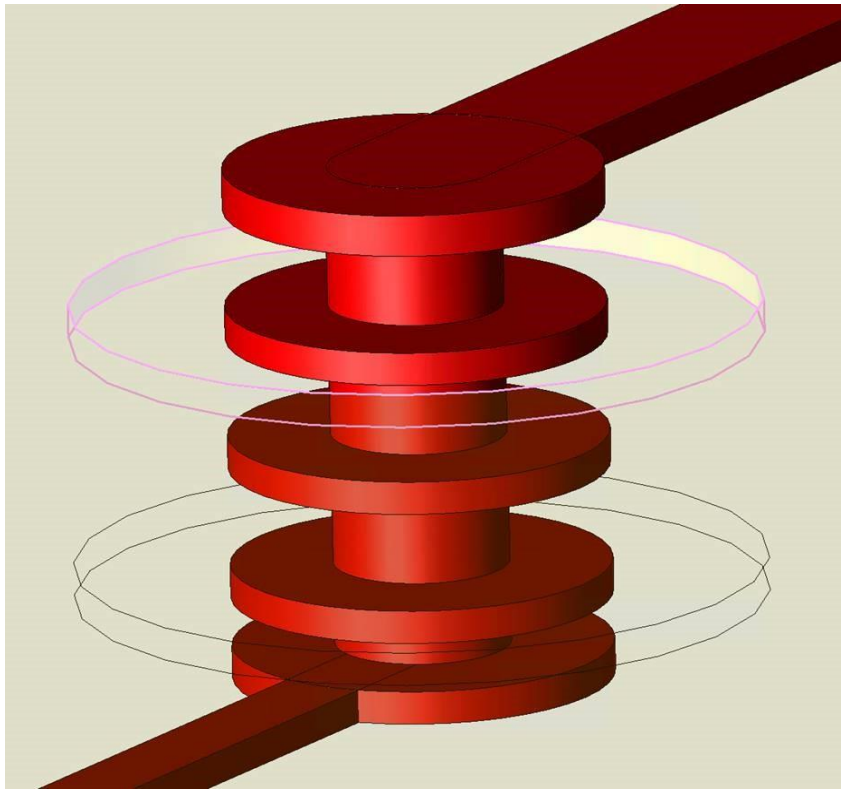
システム解析へのAI活用により解析イタレーションを削減、デザインを速やかに最適化

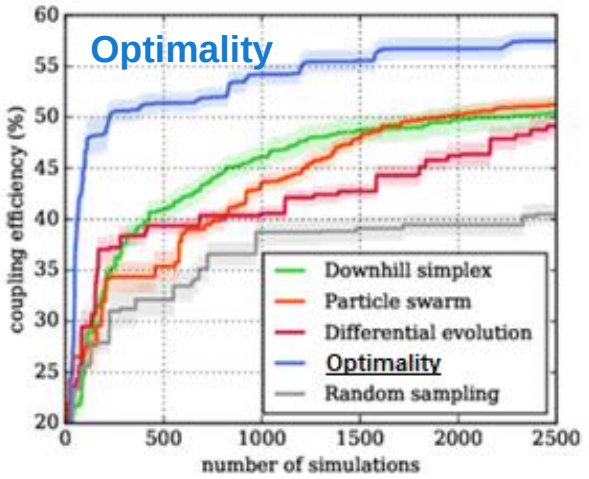


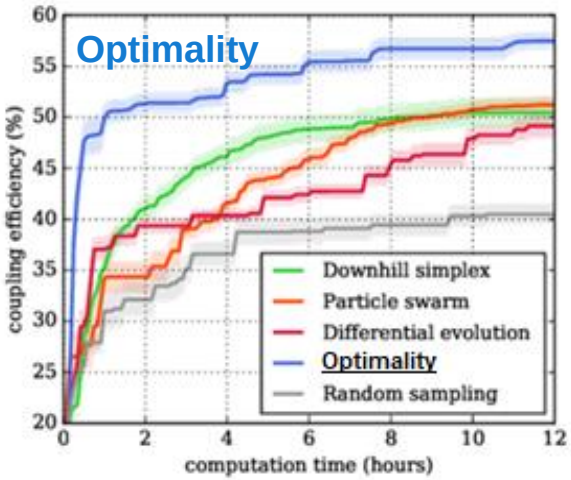
AI-driven in-design optimization

Optimality Algorithmによる最適化事例(1)

差動Viaにて結合係数要件を満たすためのPad径/Anti-Pad径最適化

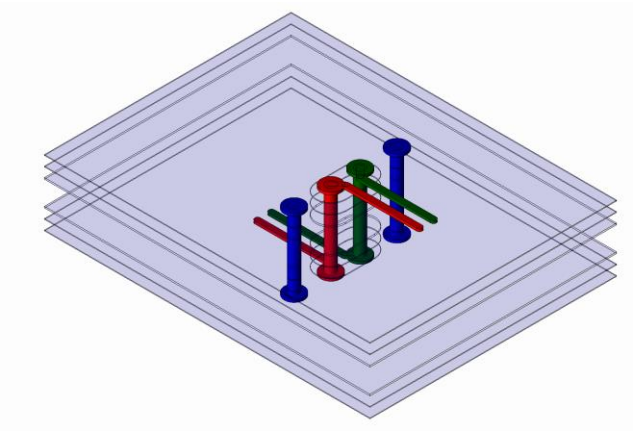


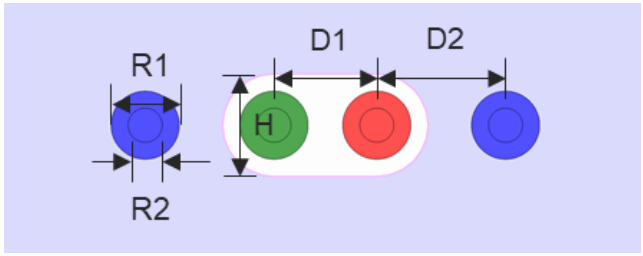




Optimality Algorithmによる最適化事例(2)

差動ViaにてReturn/Insertion Lossの要件を満たすための各種パラメータ最適化





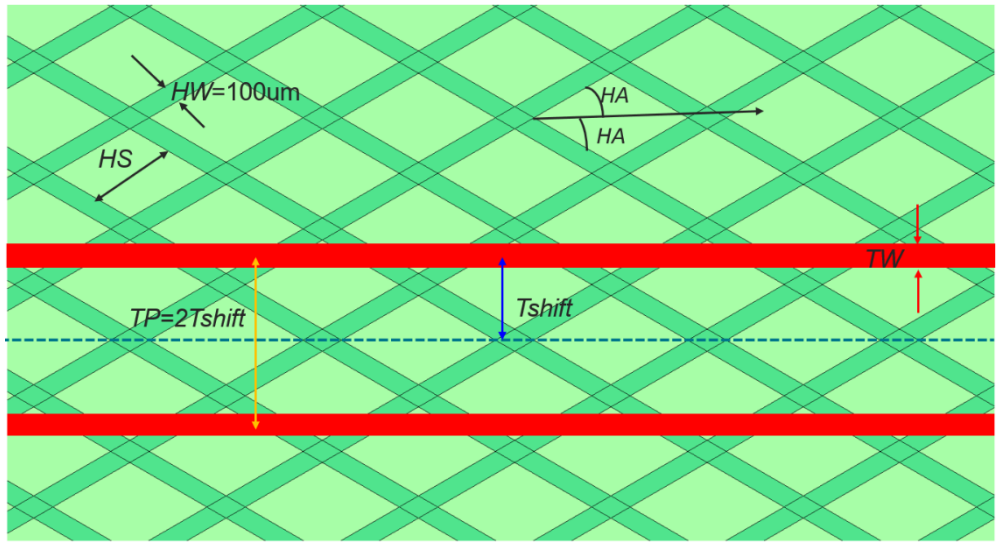
- 5 variable included in optimization
  - Diameter for Pad: R1
  - Diameter for Drill: R2
  - Height for oblong Keepout: H
  - Distance between signal Vias: D1
  - Distance between signal and gnd Vias:D2
- Goal function: differential Return/ Insertion Loss

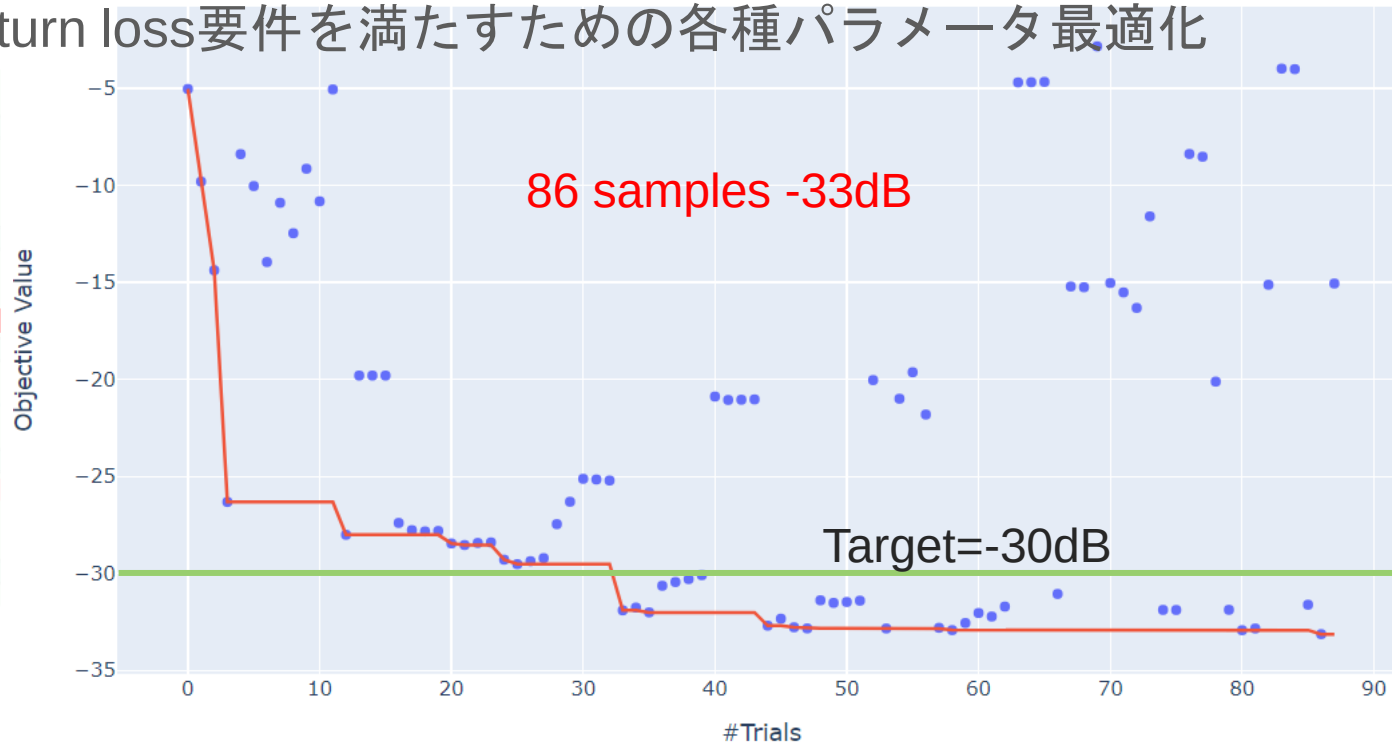
Goal	Origin (dB)	OPT (dB)	Improvement (%)
RL@5GHz	-29.4	-45.2	53.7
IL@ 5GHz	-0.14	-0.12	14.3

	Traditional Sweeping Method	Optimality Intelligent System Explorer
Computer resources	8 cores / 64GB	8 cores / 64GB
# Simulations	3125 Simulations	79 Simulations
Time comparison	**66 Hours**	**1.6 Hours**

Optimality Algorithmによる最適化事例(3)

クロスハッチプレーン間の差動ペアReturn loss要件を満たすための各種パラメータ最適化





Layer Icon	Layer Name	Thickness(mm)	Material	Er	Loss Tangent
	Plane_cross_hatch_L4	0.0175	COPPER	3.1	0.024
	Medium01	0.03		2.8	0.024
	Signal_Differential_L5	0.0175	COPPER	2.8	0.024
	Medium02	0.03		2.8	0.024
	Plane02_cross_hatch_L6	0.0175	COPPER	3.1	0.024

Optimization Target:

- Minimize Return loss:
  - -30dB in the frequency band [0GHz-15GHz]
- 4 optimization variables: *HW, HS, HA, TW, TP*
- If brute-force algorithm (sweeping) is used, total tries are 20x20x18x20x20=**2,880,000**.