ヘテロジーニアスインテグレーションGaN SiPにおけるSub-nsテスト技術

マルチチップインテグレーション調査TG
Multi Chip Integration Investigation Task Group

主査　佐藤　ローム株式会社

Introduction

What is “Heterogeneous Integration”?

Motivation of Heterogeneous Integration

❌ムーアの法則が頭打ちに

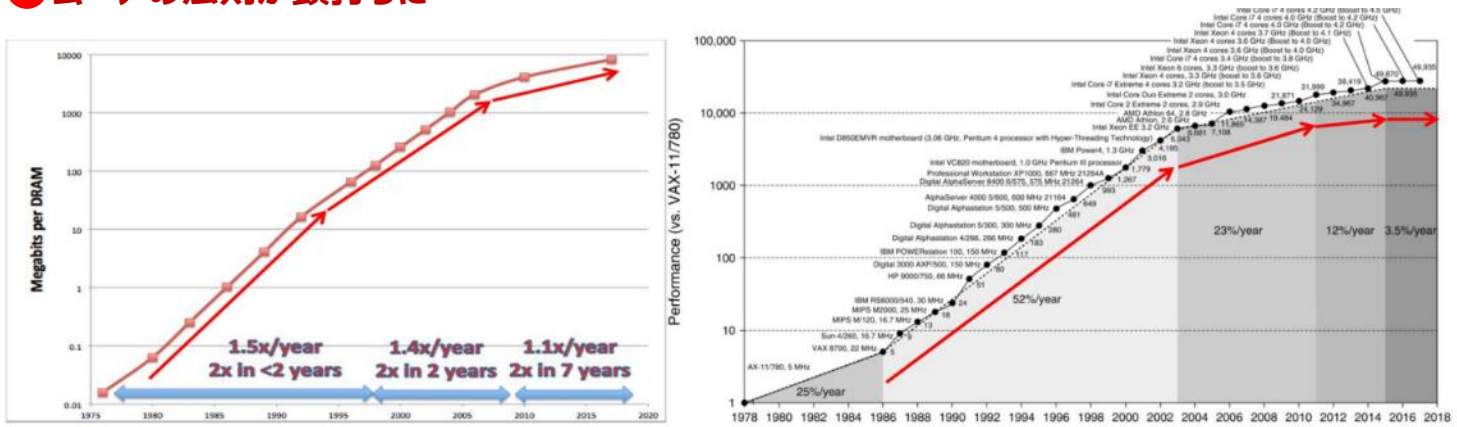
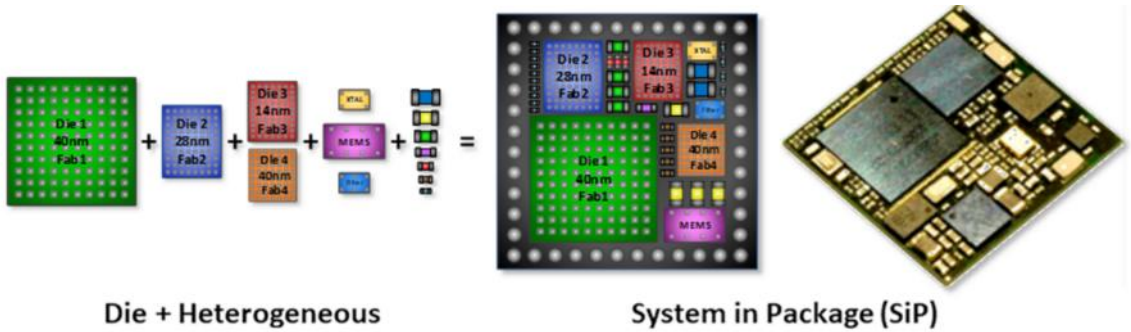


Figure 2. Plateauing of DRAM Density, and Computing Performance. Source: J Hennessy, ERI Conf July 2018

❌ 微細化によりDieコスト上昇

✅ 解決策 **Heterogeneous Integration**



Die + Heterogeneous　　System in Package (SiP)

ムーアの法則のスケーリングが遠い未来まで拡大する

Benefit

- より高いパフォーマンス
- より低いレイテンシー
- 小型化
- 軽量化
- 機能あたりの電力の低減
- 歩留まり向上によるコストの削減

出展：IEEE EPS HIR

HIR（Heterogeneous Integration Roadmap）

	CHAPTER 1	: HETEROGENEOUS INTEGRATION ROADMAP – OVERVIEW
	CHAPTER 2	: HIGH PERFORMANCE COMPUTING AND DATA CENTERS
	CHAPTER 3	: THE INTERNET OF THINGS (IOT)
	CHAPTER 4	: MEDICAL, HEALTH & WEARABLES
	CHAPTER 5	: AUTOMOTIVE
	CHAPTER 6	: AEROSPACE AND DEFENSE
	CHAPTER 7	: MOBILE
	CHAPTER 8	: SINGLE CHIP AND MULTI CHIP INTEGRATION
	CHAPTER 9	: INTEGRATED PHOTONICS
★	CHAPTER 10	: INTEGRATED POWER ELECTRONICS
	CHAPTER 11	: MEMS AND SENSOR INTEGRATION
	CHAPTER 12	: 5G COMMUNICATIONS
	CHAPTER 13	: CO DESIGN FOR HETEROGENEOUS INTEGRATION
	CHAPTER 14	: MODELING AND SIMULATION
	CHAPTER 15	: MATERIALS AND EMERGING RESEARCH MATERIALS
	CHAPTER 16	: EMERGING RESEARCH DEVICES
	CHAPTER 17	: TEST TECHNOLOGY
	CHAPTER 18	: SUPPLY CHAIN
	CHAPTER 19	: SECURITY
	CHAPTER 20	: THERMAL
★	CHAPTER 21	: SIP AND MODULE SYSTEM INTEGRATION
	CHAPTER 22	: INTERCONNECTS FOR 2D AND 3D ARCHITECTURES
	CHAPTER 23	: WAFER-LEVEL PACKAGING (WLP)
	CHAPTER 24	: Reliability
	CHAPTER 25	: Additive Manufacturing & Additive Electronics for Heterogeneous Integration(3/12Review予定)

HIR
HETEROGENEOUS
INTEGRATION ROADMAP

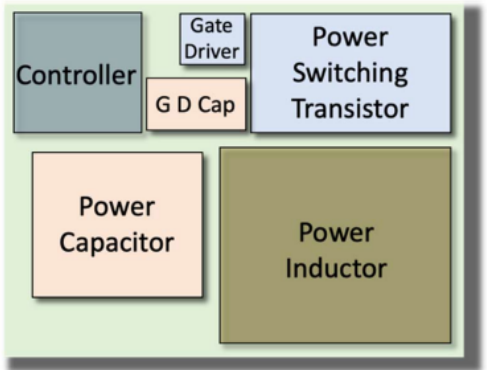
ハイライト部調査済み

出展：IEEE EPS HIR

Integrated Power Electronics Component

CHAPTER 10 : Integrated Power Electronics

Integrated Power Electronics Component (IPEC)は下図で定義される



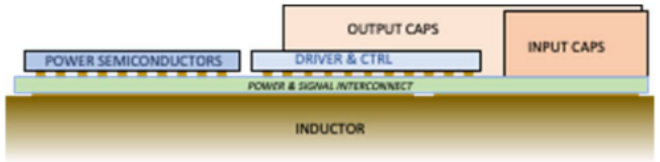
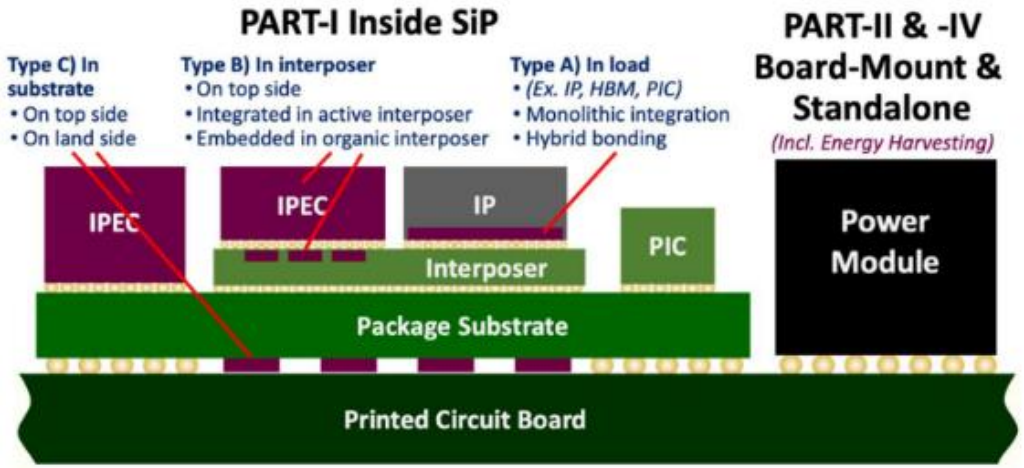
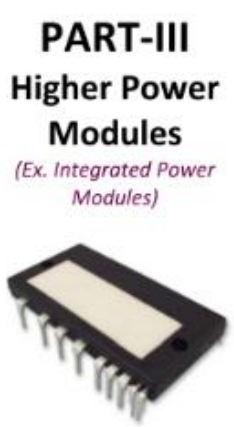


Figure 1. The "Integrated Power Electronics Component," IPEC, represents the electrical components and functions required for electronic conditioning of electrical energy delivered to the load(s). The IPECs may be partitioned and integrated in multiple ways within the System in Package, or be a standalone power electronic circuit for board-level power supply.

インダクターの上に、モジュールを構成する部品を実装したインターポーザーを設置





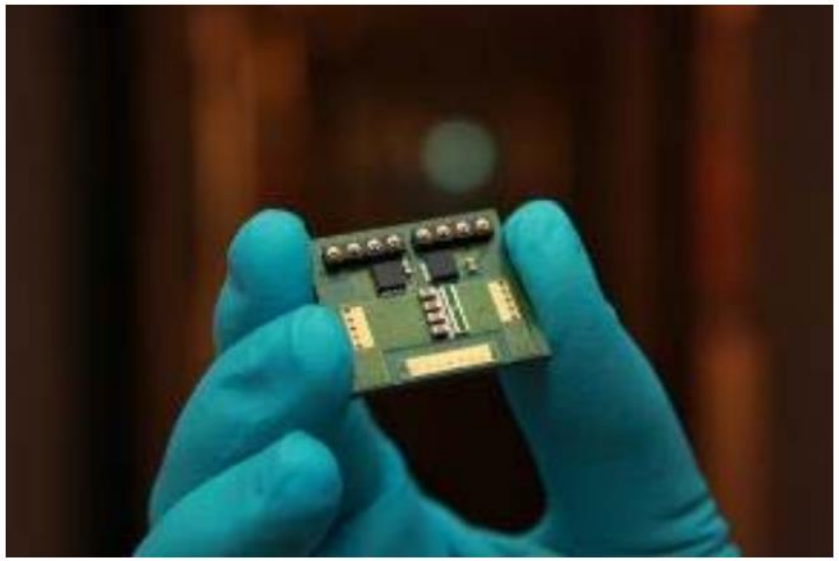
- Chapter10は、≤48V/100Aにフォーカスしている
- 基本的なテクノロジーは、はるかに高い電力レベルに適用可能

出展：IEEE EPS HIR

Heterogeneous Integration SiP Module

CHAPTER 21 : SiP and Module System Integration

Silicon carbide (SiC) and Gallium-nitride (GaN) with driver, inductor, and capacitor



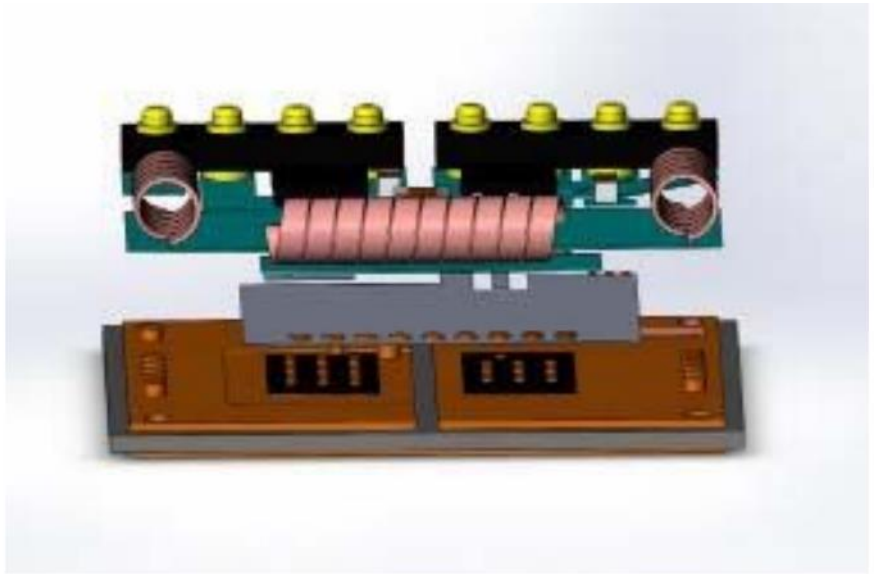


Figure 20: Example for an EMI-optimized SiC package with part of the driver and the DC-link included. [courtesy Fraunhofer IZM]

組み込みSiCモジュールの特徴

- 低い寄生インダクタンス
- 優れた高速スイッチング
- 低EMI

出展：IEEE EPS HIR

ROHM SEMICONDUCTOR

Electronics for the Future

Sub-ns Testing for Heterogeneous Integration GaN SiP

Research Objective

To achieve Sub-ns Testing for Heterogeneous Integration GaN SiP

Proposal

Development of Built-Out-Self-Test Circuit for Sub-ns Testing

Requirement

- High Accuracy
- Fast Testing
- Low Test Cost

Outline

1. Research Background
2. Sub-ns Testing
3. SAR Time-to-Digital Converter
   - Principle
4. Vernier SAR Time-to-Digital Converter
   - Principle
   - Verification
   - Experiment
5. Trial using GaN Gate Driver
6. Conclusion

1. Research Background

The GaN has attracted much attention in recent years

High Energy efficiency is required

GaN AC Adapter

EcoGaN

Characteristic

✓High Voltage and Low Loss

✓Heat Resistant

✓High Frequency Drive

The GaN has great potential for further energy savings

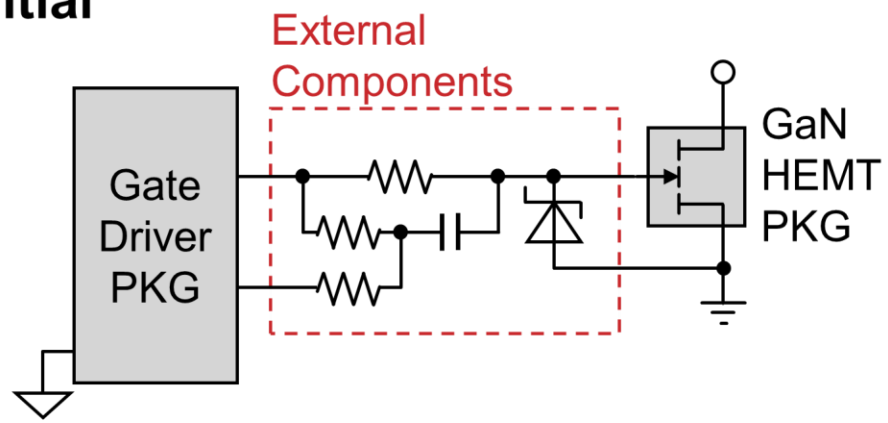
1. Research Background

The difficulty of using GaN

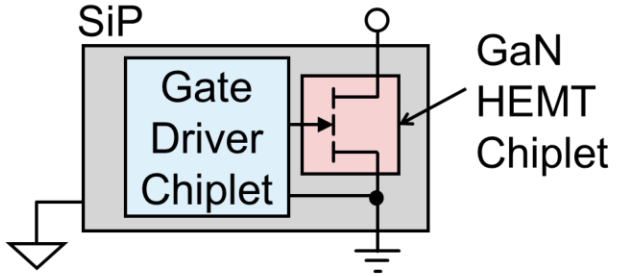
- Narrow drive voltage range Risk : Self turn-on
- Low gate withstand voltage Risk : Gate breakdown
- Need exclusive Gate Driver IC and external components

Solution

Initial



Heterogeneous Integration

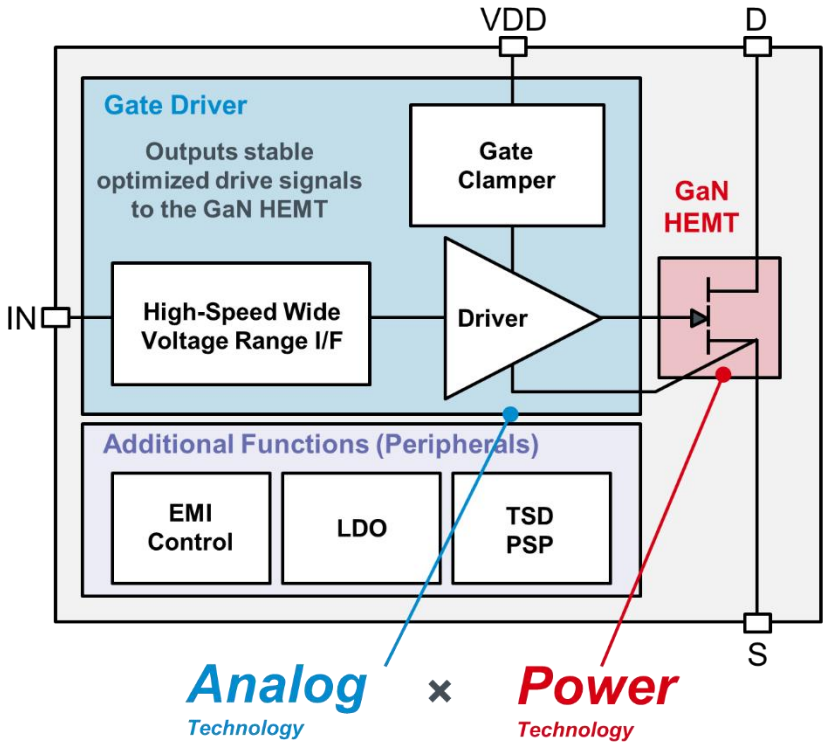


Heterogeneous Integration is required

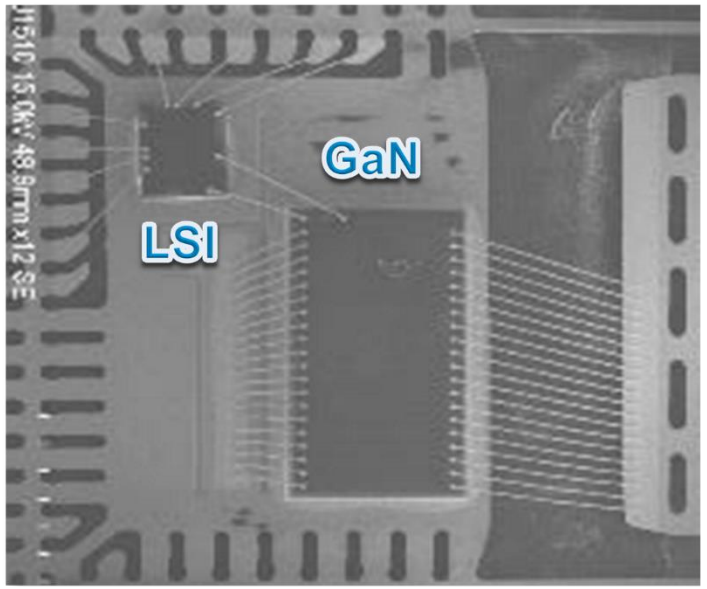
1. Research Background

Heterogeneous Integration GaN SiP

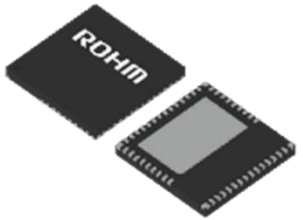
BM3G0xxMUV-LB series Block Diagram



GaN SiP



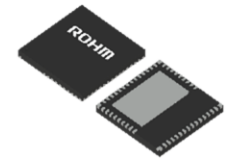
VQFN046V8080
8.0mm x 8.0mm x 1.0mm
pitch 0.5mm



Heterogeneous Integration GaN SiP will maximize GaN HEMT performance

1. Research Background

650V GaN HEMT Power Stage SiP

Part No.	Drain Pin Voltage (Max) [V]	Input Voltage Range [V]	Supply Pin Voltage [V]	Supply Pin Operating Current (Typ) [μA]	Supply Pin Quiescent Current (Typ) [μA]	ON Resistance (Typ) [mΩ]	Turn ON Delay Time (Typ) [ns]	Turn OFF Delay Time (Typ) [ns]	Operating Temperature Range [°C]	Package
BM3G015MUV-LB	650	-0.6 to +30	6.25 to 30	450	150	150	11	15	-40 to +105	 VQFN046V8080 (8.0×8.0×1.0mm)
BM3G007MUV-LB				650	180	70	12			

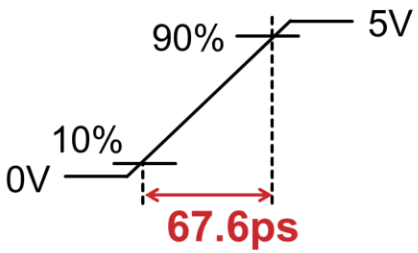
Click on the icon to access the product page on ROHM's website. Click on the icon to access the product datasheet on ROHM's website.

Sub-ns Testing

■ **Rise Time**

16.9ps/V

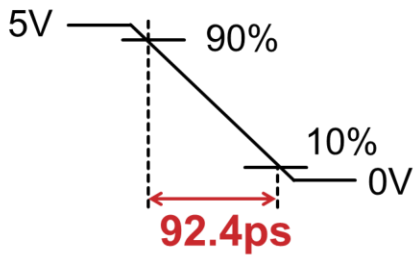
(11ns/650V)



■ **Fall Time**

23.1ps/V

(15ns/650V)



±1ps resolution is required for mass production testing

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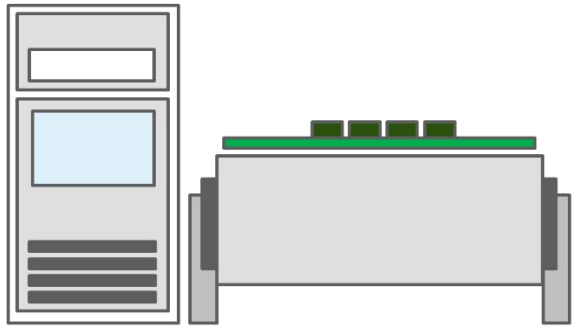
2. Sub-ns Testing

Conventional Method

Use of External Instruments

Low-end ATE



+

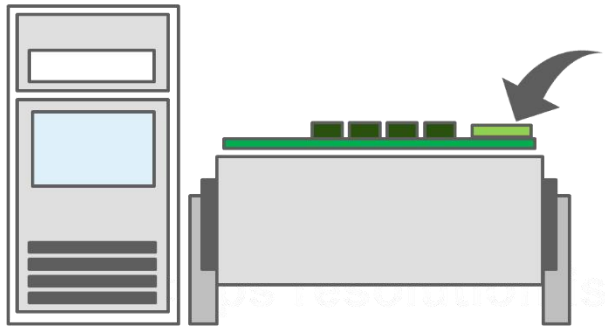
Tektronix® MSO5xB
6.25GS/s, 2GHz Band Width

- ✅ High Accuracy
- ❌ Fast Testing
- ❌ Low Test Cost

Proposed Method

Use of BOST Circuit

Low-end ATE



Development of BOST Circuit

High accuracy time measurement

- ❓ High Accuracy (±1ps)
- ❓ Fast Testing
- ❓ Low Test Cost

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Sorry

No distribution

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6. Conclusion

To achieve Sub-ns Testing for Heterogeneous Integration GaN SiP

Development of BOST Circuit

- Vernier SAR Time-to-Digital Converter achieves ±1 ps resolution
- Gaussian Noise is effective for vernier scale

Achievement

- High Accuracy : Resolution is ±1 ps
- Fast Testing : Test time is less than 30 ms w/ 512 times sampling
- Low Test Cost : No external instruments required

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