

Effective simulation set up with latest IBIS models

cooperation with IEC 63055 / IEEE 2401

Yoshinori Fukuba (JEITA, TOSHIBA)

Kazuki Murata (JEITA, Ricoh)

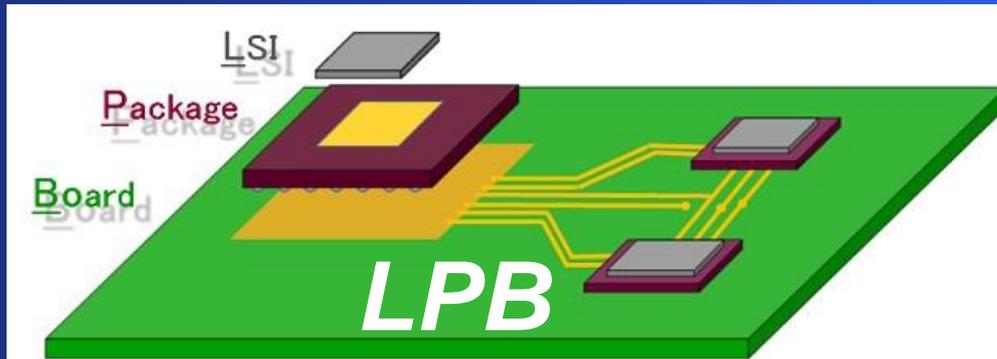
LSI Package Board needs...

- ✦ Mutual Communication
- ✦ Design Consistency
- ✦ Shorten Development Time

Enabled by



and **LPB** Standard formats



Contents

- Introduction
 - Background of technology matters
 - What is IEC 63055/ IEEE 2401?
 - JEITA delegates & History of discussion IBIS and JEITA
- Technical aspect between IBIS and IEC 63055/ IEEE 2401
 - Issues on IBIS simulation
 - Automated setup of IBIS simulation – How IEEE 2401 does help. Benefits.
 - Sample of IEEE 2401, sample of IBIS simulation set up
 - Concerns and required actions.
- Conclusion & Proposal

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 - Sample of IEEE 2401, sample of IBIS simulation. set up
 - Concerns and required actions.
- Conclusion & Proposal
 - Joint work for harmonization with latest IBIS and IEEE 2401 (and future)
 - IEEE 2401-2020 update – join P2401 working group if you are IEEE-SA member

Background of technology matters

In Technical, Increasing of connected node causes the long time work,

- Conversion work from someone's info. To someone's work environment
- Mistakes may occur in manual connection, but just watching the results, mistake cannot be detected.
- As a results, it takes long time for verification work to correct setup

Engineer's valuable time is lost in such a wasteful work. Engineers have to spend time for innovation.

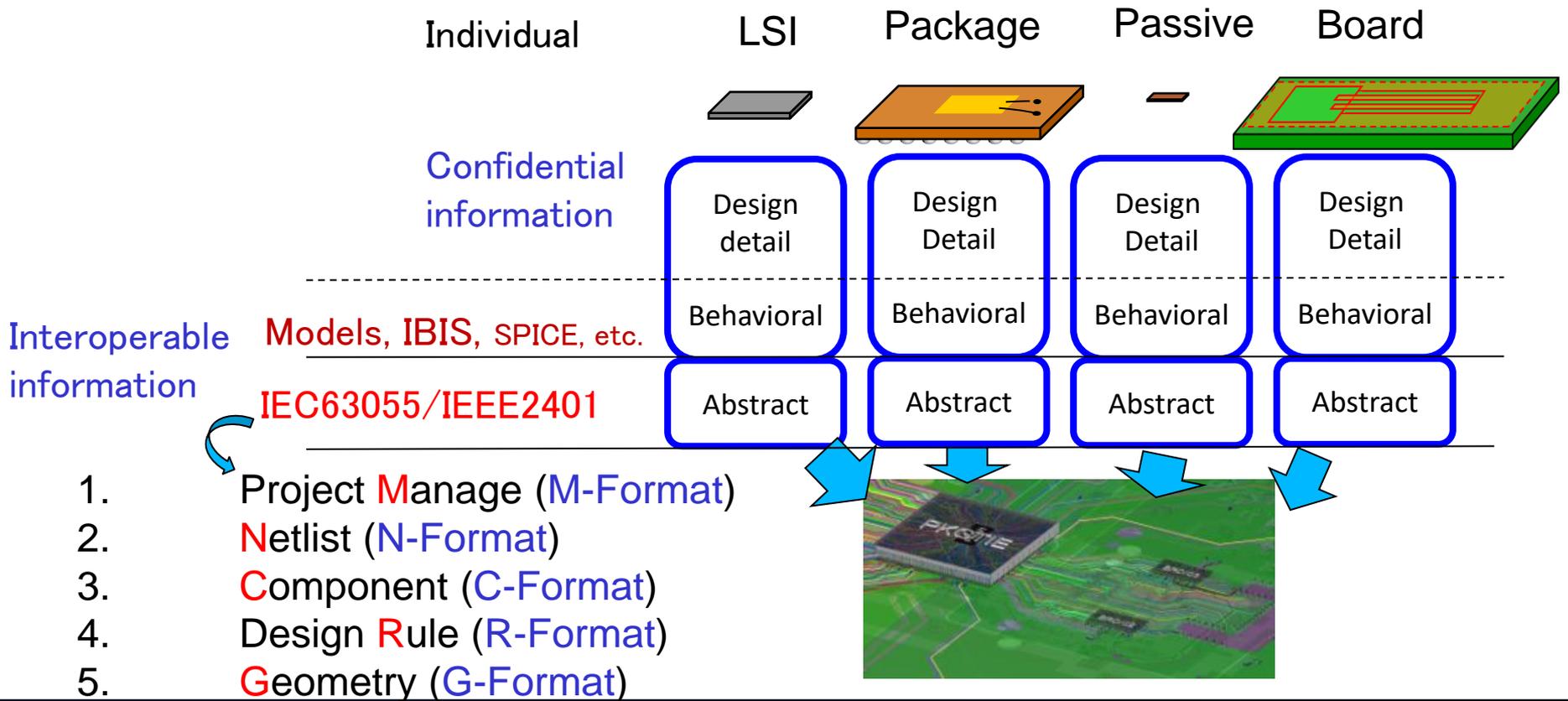
In Business, delay to put the product in market.

Design technology leads to business success.

What is IEC 63055/ IEEE 2401-2015?

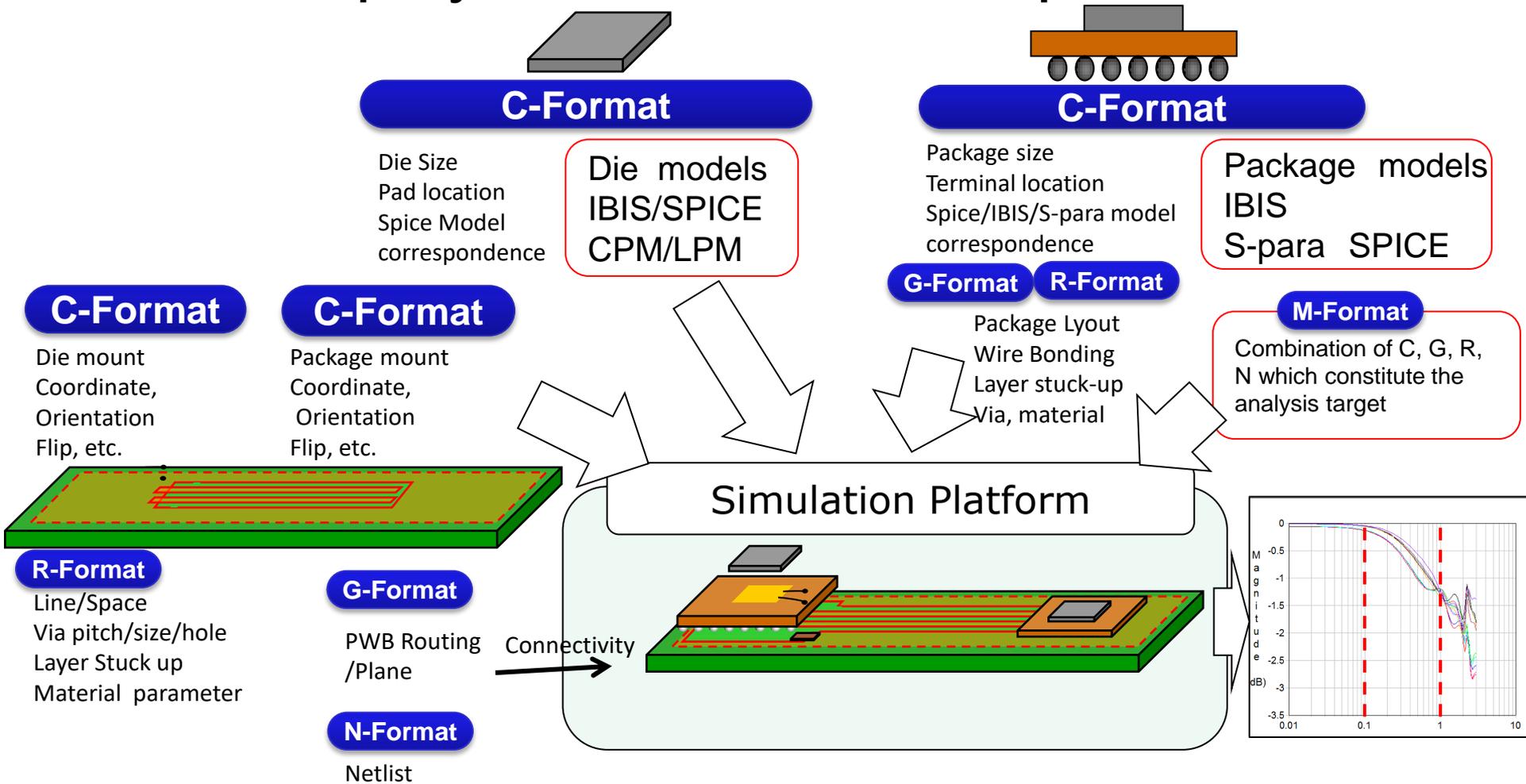
Standard format for **L**SI **P**ackage **B**oard (LPB)
interoperable design.

For effective information exchange in supply chain.



What is IEC 63055/ IEEE 2401-2015?

In the deployment of electronic products...



Delegates of JEITA



JEITA

Japan Electronics and Information Technology Industries Association

Japan Electricals and Information Technology Industries Association



JEITA-JSIA

Semiconductor Industry Association in Japan

Semiconductor Standardization Committee in Japan



LPB

Semiconductor & System Design Technical Committee

Chair : Yoshinori Fukuba (from Toshiba)



LPB

LPB(LSI Package board) interoperable design sub-committee

LPB modeling Working Group / IBIS Task Group

Leader: Kazuki Murata (From Ricoh)



**JEITA
EC CENTER**

• IBIS Summit Japan coordinator



LPB

<http://jeita-sdtec.com/worldwide/>

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History of IBIS & LPB

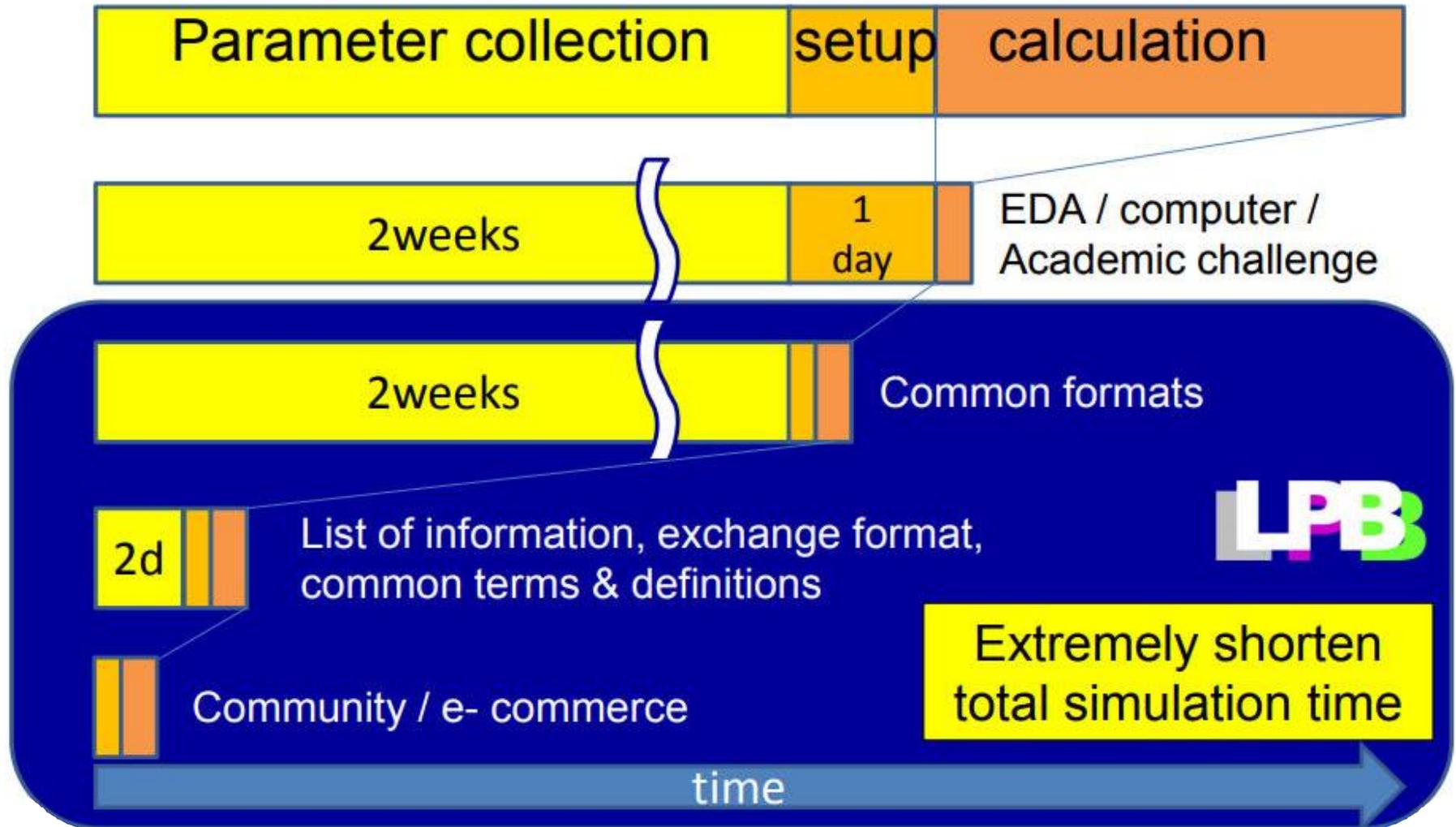
1. 2013 Asian IBIS Summit Yokohama, Mr. Murata presented on V5.x, AMI's consideration. After that Fukuba talked with Mr. Michael Mirmak, former chairperson IBIS Open Forum, about the cooperation between IBIS & LPB.
2. Mr. Tanaka introduced LPB concept at 2014 IBIS Summit @ DAC (San Francisco)
3. Fukuba presented LPB concept at 2015 Asian IBIS Summit Yokohama (almost the same content as Mr. Tanaka's)
4. Mr. Murata presented the chip model at 2017 Asian IBIS Summit Akihabara, Tokyo, after that Fukuba discussed cooperative relationship with Mr. Mike LaBonte.



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Overall Simulation time



Waste of time – Pin connection

It is complicated to assign IBIS model to component in board layout data.

Too many [Pin]s to connect manually!

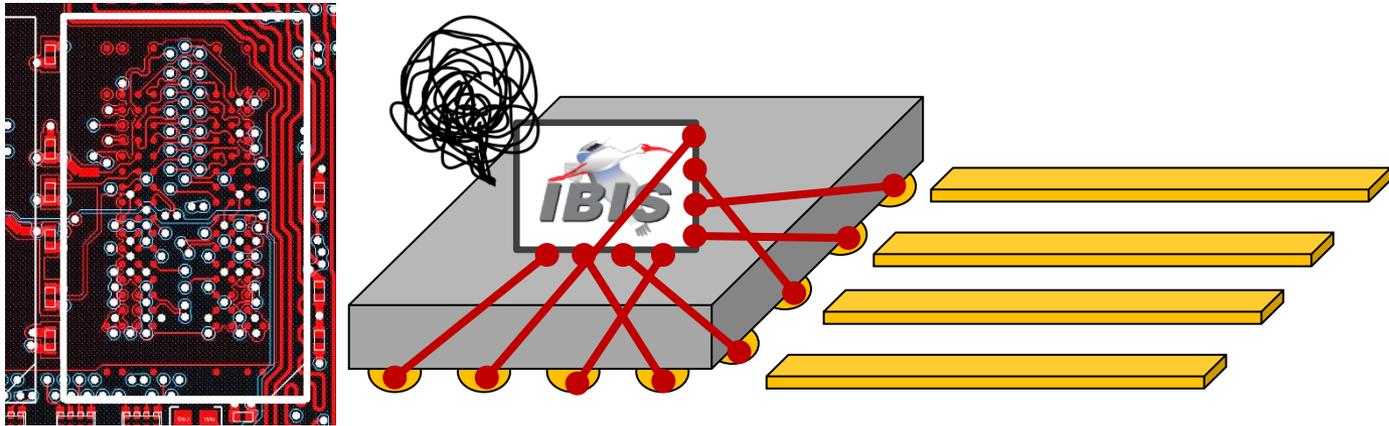
Example: number of pins.

DDR4 64bit	FPGA-A	FPGA-B	SoC-A	SoC-B
114	2892	2912	1760	2597

Some tools can connect them automatically.

But, we can't always get correct result by keyword matching method.

Is [Pin] name physical pin name? A1,A2,A3,B1,,,



LPB - Explicit connection

LPB can contains the correspondence of IBIS [Pin] to chip pin's physical position.

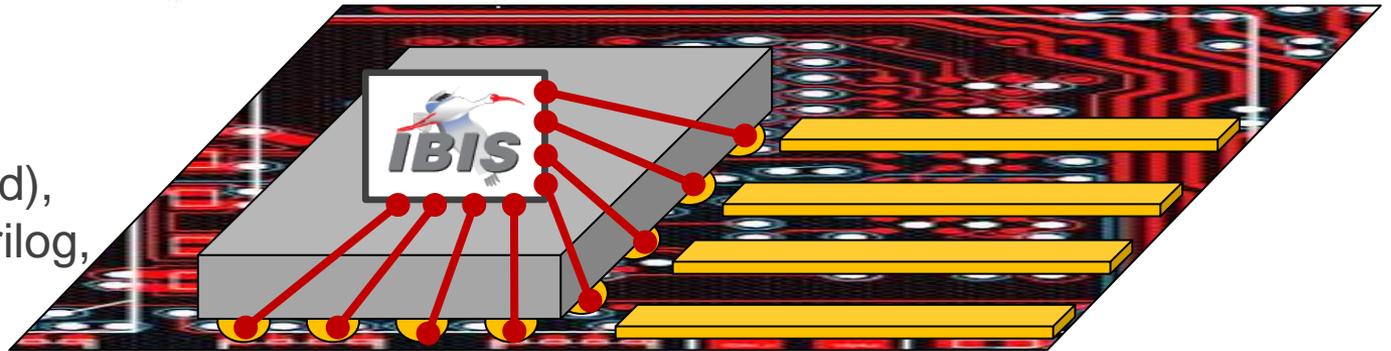
LPB

```
- <socket name="DDR3_x16_sdp_socket">
  <port name="VDDQ" angle="0" y="6000" x="-3200" direction="inout" type="power" id="A1"/>
  <port name="DQU5" angle="0" y="6000" x="-2400" direction="inout" type="signal" id="A2"/>
  <port name="DQU7" angle="0" y="6000" x="-1600" direction="inout" type="signal" id="A3"/>
</socket>
- <reference reffile="dram.ibs" format="IBIS" xmlns:ibis="http://www.jeita.or.jp/LPB/ibis">
  - <connection port_id="A1" socket_name="DDR3_x16_sdp_socket">
    <ibis:ref_port pin_name="A1" component="AA512M16BB"/>
  </connection>
  - <connection port_id="A2" socket_name="DDR3_x16_sdp_socket">
    <ibis:ref_port pin_name="A2" component="AA512M16BB"/>
  </connection>
  - <connection port_id="A3" socket_name="DDR3_x16_sdp_socket">
    <ibis:ref_port pin_name="A3" component="AA512M16BB"/>
  </connection>
</reference>
```

Physical position

Link LPB <port> to IBIS [Pin]

LPB supports
IBIS(.ibs, .pkg, .ebd),
SPICE, Spara, Verilog,
etc.



Waste of time – Data conversion

SI/PI/EMC designers have to use various tools.

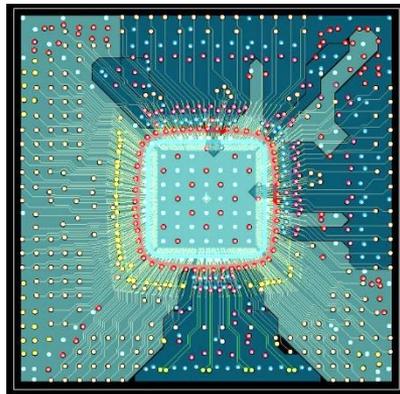
for die tools, for PKG tools, for Board tools, simulators, CAD,,,

Therefore it is necessary to convert the data many times.

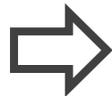
Format A -> Format B -> Format C

Are A and C the same layout?

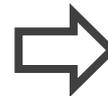
It is complicated to modify the data manually to be the same.



Designed by
PKG Planning tool



Via
Layout tool data format

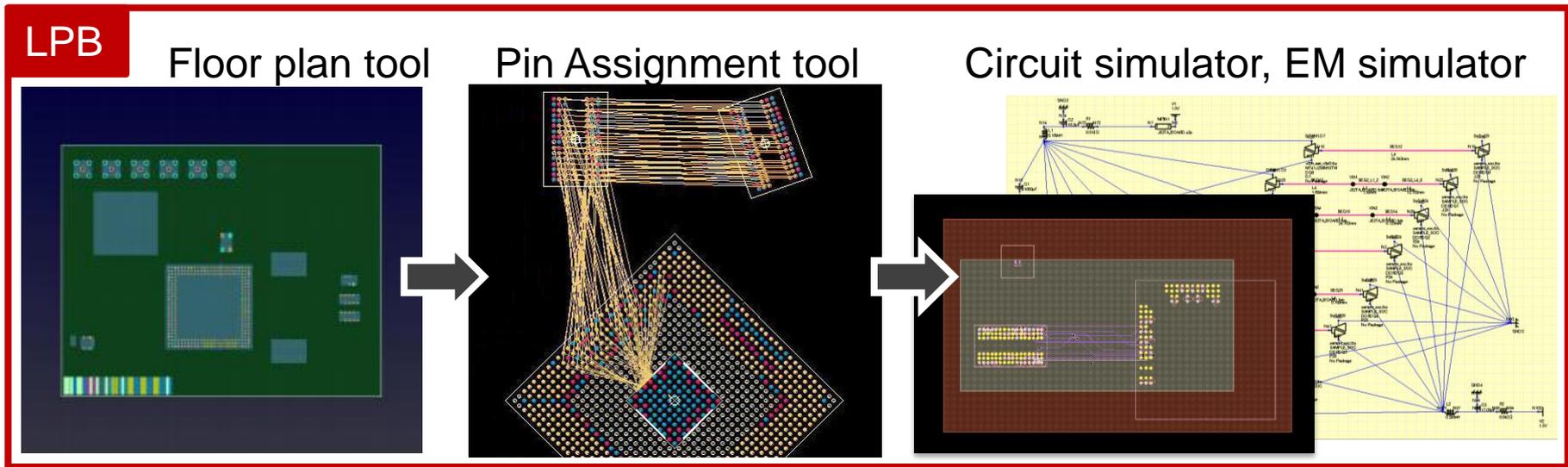


Simulation by
EM simulator

LPB - Seamless design

LPB is mainly XML format, and IEC and IEEE standard.

Various tools support LPB. Therefore data conversion is unnecessary.



LPB has module's physical shape data and layout data.

die outline, PKG outline, die pad shape, PKG ball shape, etc.

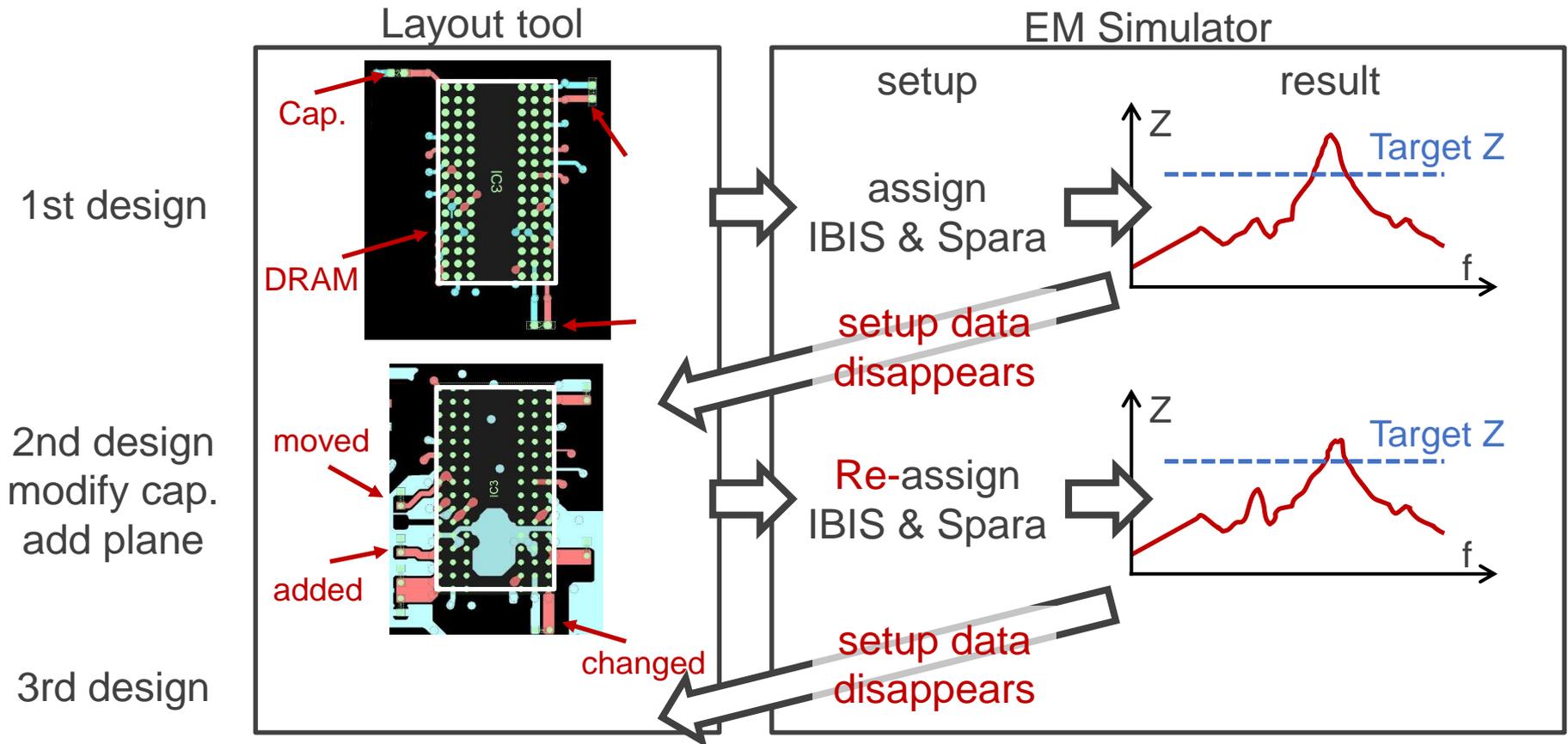
P/G plane shape, transmission line shape, layer stackup, etc.

And, these modules are linked to IBIS models or other models.

LPB makes it easy to proceed design phase.

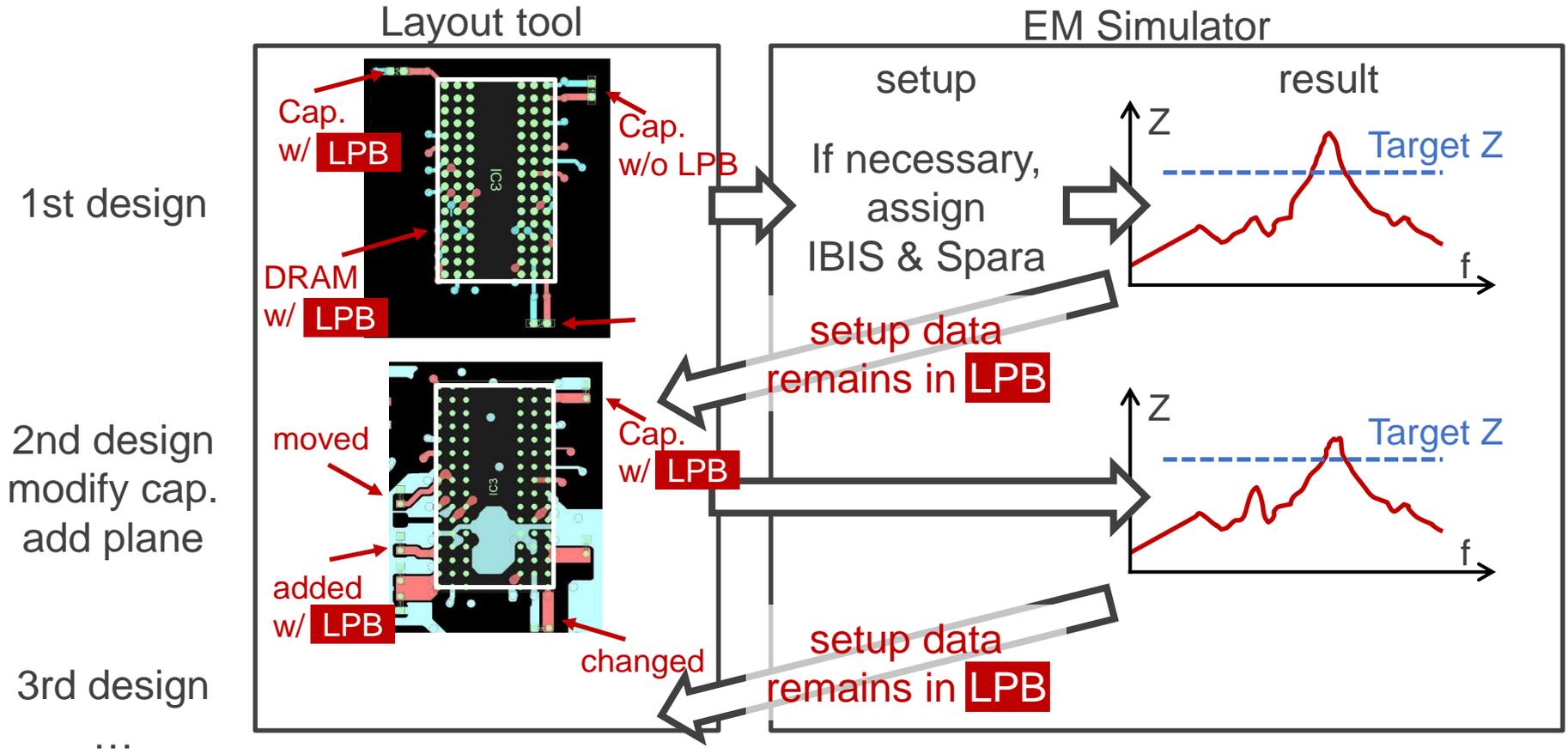
Waste of time – Re-setup

Board layout changes may be occurred many times during design phase.
SI/PI/EMC designers also have to do simulation many times.

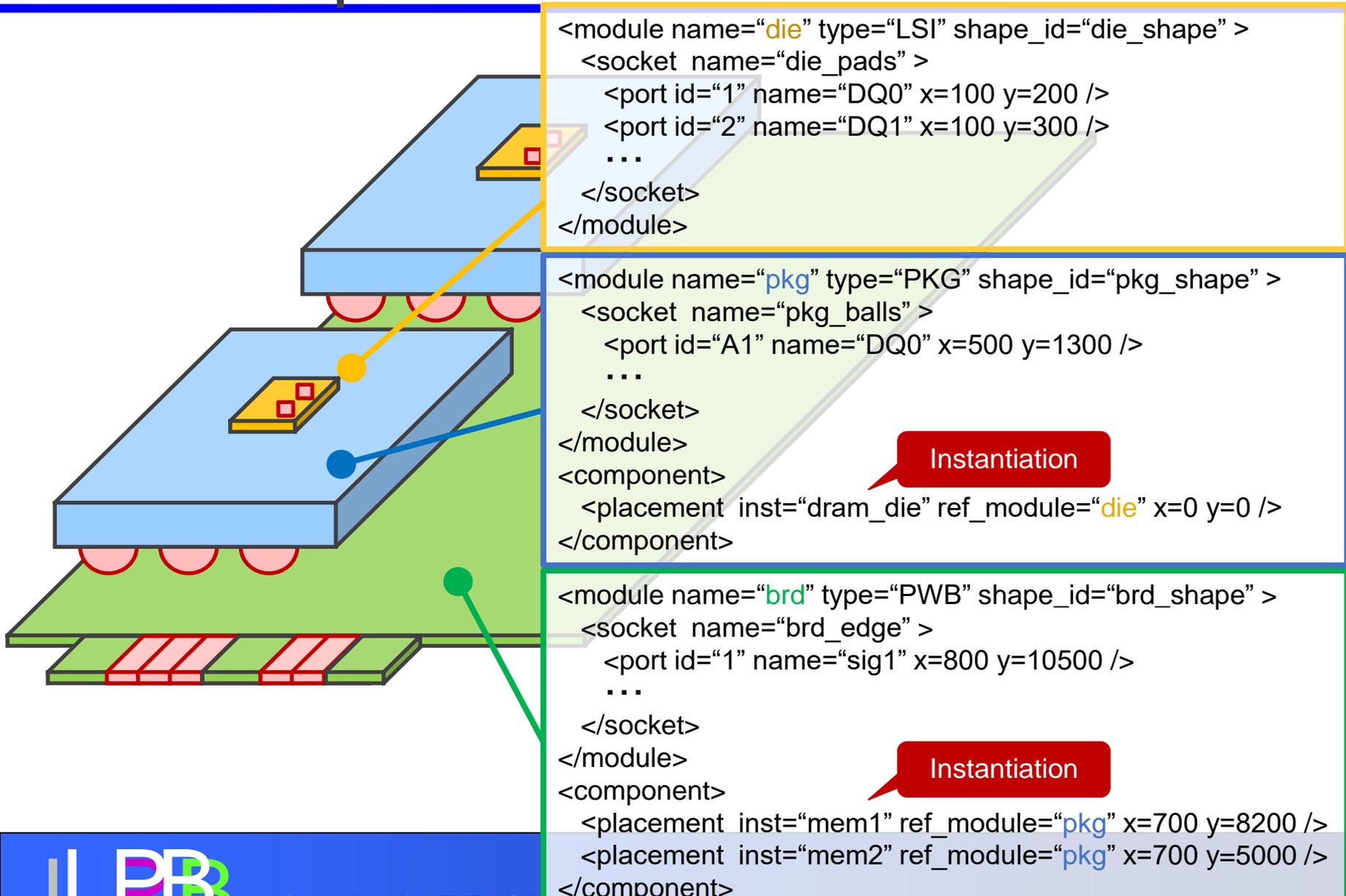


LPB – Setup iteration-free

Once you setup simulation by using LPB, you can reuse it **without re-setup**.



Example of LPB



```
<module name="die" type="LSI" shape_id="die_shape" >  
  <socket name="die_pads" >  
    <port id="1" name="DQ0" x=100 y=200 />  
    <port id="2" name="DQ1" x=100 y=300 />  
    ...  
  </socket>  
</module>
```

```
<module name="pkg" type="PKG" shape_id="pkg_shape" >  
  <socket name="pkg_balls" >  
    <port id="A1" name="DQ0" x=500 y=1300 />  
    ...  
  </socket>  
</module>  
<component>  
  <placement inst="dram_die" ref_module="die" x=0 y=0 />  
</component>
```

Instantiation

```
<module name="brd" type="PWB" shape_id="brd_shape" >  
  <socket name="brd_edge" >  
    <port id="1" name="sig1" x=800 y=10500 />  
    ...  
  </socket>  
</module>  
<component>  
  <placement inst="mem1" ref_module="pkg" x=700 y=8200 />  
  <placement inst="mem2" ref_module="pkg" x=700 y=5000 />  
</component>
```

Instantiation

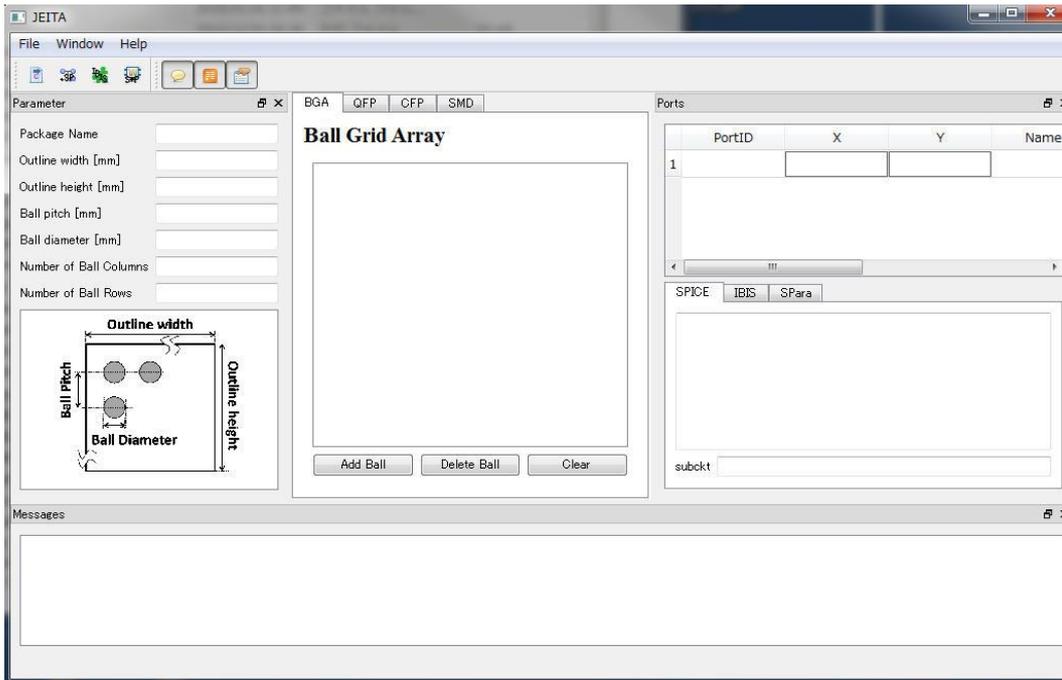
Who provides LPB?

For the components, LPB files should be released by component vendors.

Some commodity parts are getting ready!

JEITA has released the sample data and tools for either vendor or user to create LPB files.

In case you have to make LPB by yourself, use 'LPB design kit' released by JEITA that can export simple LPB files.



<http://www.lpb-forum.com/lpb-open-source-project/download/>
Sorry, this web site is Japanese.

How to make LPB with IBIS

Example: DRAM

Import IBIS

[Pin]

IBIS Viewer

[Component]

Parameter

Package Name	DRAM
Outline width [mm]	9
Outline height [mm]	14
Ball pitch [mm]	0.8
Ball diameter [mm]	0.45
Number of Ball Columns	9
Number of Ball Rows	16

Ball Grid Array

	1	2	3	4	5	6	7	8	9
A	o	o	o				o	o	o
B	o	o	o				o	o	o
C	o	o	o				o	o	o
D	o	o	o				o	o	o
E	o	o	o				o	o	o
F	o	o	o				o	o	o
G	o	o	o				o	o	o
H	o	o	o				o	o	o
I	o	o	o				o	o	o
J	o	o	o				o	o	o
K	o	o	o				o	o	o
L	o	o	o				o	o	o
M	o	o	o				o	o	o
N	o	o	o				o	o	o
O	o	o	o				o	o	o
P	o	o	o				o	o	o

Ports

PortID	X	Y	Name	Direction	Type	IBIS	
1	A1	-3.2	-6.0	VDD_DDR	inout	power	A1
2	A2	-2.4	-6.0	VSS_DDR	inout	ground	A2
3	A3	-1.6	-6.0	DQ8	inout	signal	A3
4	A4	-0.8	-6.0				
5	A5	0.0	-6.0				
6	A6	0.8	-6.0				
7	A7	1.6	-6.0	DQS1N	inout	signal	A7
8	A8	2.4	-6.0	VSS_DDR	inout	ground	A8

IBIS Viewer

```
[Component] MM512M16
[Package Model] dram_96ball_pkg
[Manufacturer] JEITA_sample
[Package]
|
| typ min max
R_pkg 389.47m 340.46m 429.25m
L_pkg 1.78nH 1.30nH 2.35nH
C_pkg 0.42pF 0.32pF 0.74pF
|
| [Pin] signal_name model_name R_pin L_pin C_pin
A1 VDDQ POWER
A2 VSSQ GND
A3 DQ8 DQ 346.42m 1.32nH 0.42pF
A7 UDQS_c DQS 359.83m 1.34nH 0.41pF
A8 VSSQ GND
```

component MM512M16

How to make LPB with IBIS

Example: DRAM

Export LPB

Parameter

Package Name: DRAM

Outline width [mm]: 9

Outline height [mm]: 14

Ball pitch [mm]: 0.8

Ball diameter [mm]: 0.45

Number of Ball Columns: 9

Number of Ball Rows: 16

Ball Grid Array

	1	2	3	4	5	6	7	8	9
A	o	o	o				o	o	o
B	o	o	o				o	o	o
C	o	o	o				o	o	o
D	o	o	o				o	o	o
E	o	o	o				o	o	o
F	o	o	o				o	o	o
G	o	o	o				o	o	o
H	o	o	o				o	o	o
I	o	o	o				o	o	o
J	o	o	o				o	o	o
K	o	o	o				o	o	o
L	o	o	o				o	o	o
M	o	o	o				o	o	o
N	o	o	o				o	o	o
O	o	o	o				o	o	o
P	o	o	o				o	o	o

Diagram showing Outline width, Outline height, Ball Pitch, and Ball Diameter.

LPB

```
<JEITA_LPB_CFORMAT version="2.2">
<header date="" design_revision="" project="" />
<global>
<unit>
<distance unit="mm" />
<time unit="ps" />
<angle unit="degree" />
</unit>
<shape>
<rectangle height="14.0" id="1" width="9.0" />
<circle diameter="0.45" id="2" />
</shape>
<padstack_def>
<padstack id="1">
<ref_shape pad_layer="BOTTOM" shape_id="2" x="0" y="0" />
</padstack>
</padstack_def>
</global>
<module name="DRAM" shape_id="1" thickness="0" type="PKG" x="0" y="0">
<socket name="socket">
<default>
<port_shape padstack_id="1" />
</default>
<port direction="inout" id="A1" name="VDD_DDR" type="power" x="-3.2" y="-6.0" />
<port direction="inout" id="A2" name="VSS_DDR" type="ground" x="-2.4" y="-6.0" />
<port direction="inout" id="A3" name="DQ8" type="signal" x="-1.6" y="-6.0" />
<port direction="inout" id="A7" name="DQS1N" type="signal" x="1.6" y="-6.0" />
<port direction="inout" id="A8" name="VSS_DDR" type="ground" x="2.4" y="-6.0" />
</socket>
<reference format="IBIS" reffile="dram_sample.ibs" xmlns:ibis="http://www.jeita.or.jp/LPB/ibis" />
<connection socket_name="socket" port_id="A1">
<ibis:ref_port component="MM512M16" pin_name="A1" />
</connection>
<connection socket_name="socket" port_id="A2">
<ibis:ref_port component="MM512M16" pin_name="A2" />
</connection>
<connection socket_name="socket" port_id="A3">
<ibis:ref_port component="MM512M16" pin_name="A3" />
</connection>
<connection socket_name="socket" port_id="A7">
<ibis:ref_port component="MM512M16" pin_name="A7" />
</connection>
<connection socket_name="socket" port_id="A8">
<ibis:ref_port component="MM512M16" pin_name="A8" />
</connection>
</module>
</global>
</CFORMAT>
```

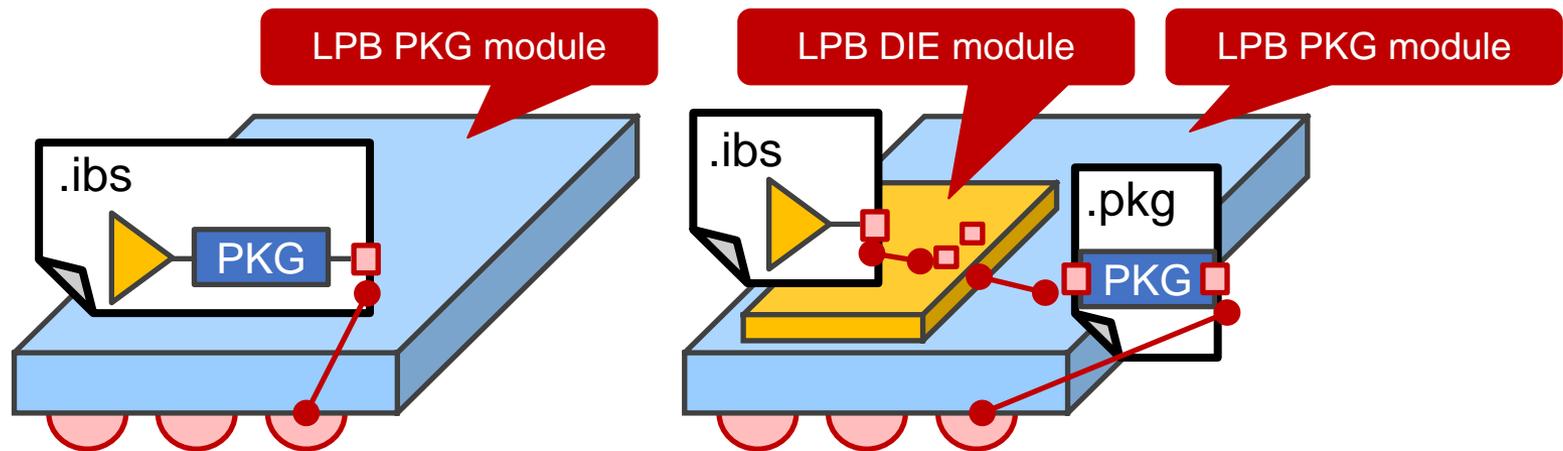
with IBIS

Save Cancel

Study for IBIS & LPB, Case: IBIS 6.0

In many cases, **IBIS6.0 doesn't have die pad information.**
Therefore IBIS is linked to LPB PKG module.

If you obtain .pkg file and .ibs file without package model, you can use them for PKG module and DIE module separately.
Then PKG module can be stacked with DIE module.



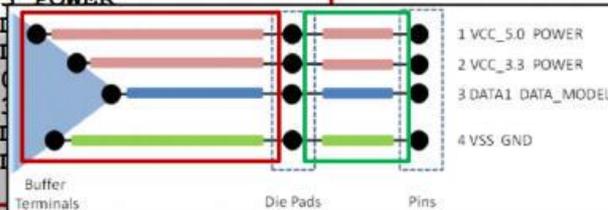
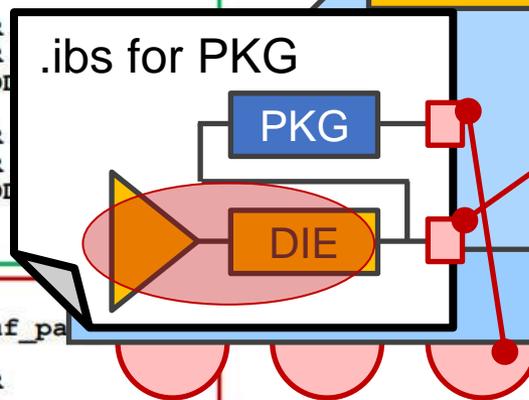
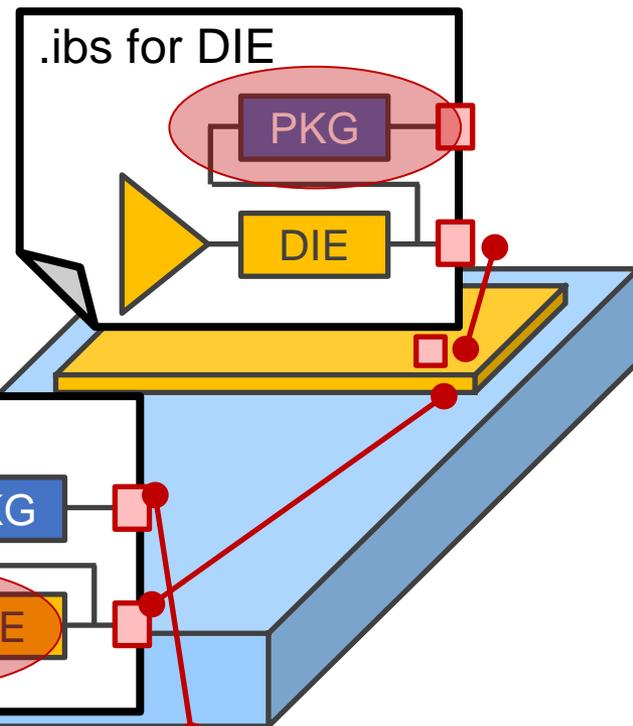
Study for IBIS & LPB, Case: IBIS 7.0

[Interconnect Model] can define die pad.
In this case LPB DIE module may be available.

But, there is a possibility that the tool recognizes each model twice – **double counting problem**.

```
[Interconnect Model]
Full_ISS_pad_pin_IO
File_IBIS-ISS full_pad_pin_io.iss full_pad_pin_IO_typ
Number of terminals = 8
1 Pin_Rail pin_name 1 | VCC_5.0 POWER
2 Pin_Rail pin_name 2 | VCC_3.3 POWER
3 Pin_I/O pin_name 3 | DATA1 DATA_MODEL
4 Pin_Rail pin_name 4 | VSS GND
5 Pad_Rail → pad_name VCC1 | VCC_5.0 POWER
6 Pad_Rail → pad_name VCC2 | VCC_3.3 POWER
7 Pad_I/O pin_name 3 | DATA1 DATA_MODEL
8 Pad_Rail → pad_name VSS1 | VSS GND
[End Interconnect Model]
```

```
[Interconnect Model]
Full_ISS_buf_pad_IO
File_TS full_buf_pad_io.s8p | full_buf_pa
Number of terminals = 8
1 Pad_Rail → pad_name VCC1 | VCC_5.0 POWER
2 Pad_Rail → pad_name VCC2 | VCC_3.3 POWER
3 Pad_I/O pin_name 3 | DATA1
4 Pad_Rail → pad_name VSS1 | VSS GND
5 Buffer_Rail pin_name 1 | VCC_5.0
6 Buffer_Rail pin_name 2 | VCC_3.3
7 Buffer_I/O pin_name 3 | DATA1
8 Buffer_Rail pin_name 4 | VSS GND
[End Interconnect Model]
```



'IBIS Update' Mike LaBonte Nov. 17 2017 Asian IBIS Summit in Tokyo

Concerns and required actions

Concern: double count of die and PKG model in case LPB with IBIS7.0

Action: add the optimal function to LPB ?

 active

LPB		[Model]	[Package]	[Pin]	[Package Model]	[Inter-connect]
Example of modification to correspond to IBIS 7.0						
<ibis:ref_port component=aaa />			(Depends on simulator)	
	<pkg type=short/>					
	<pkg type=package/>					
	<pkg type=pin/>					
	<pkg type=package_model/>					
	<interconnect name=xxx/>					
<ibis:ref_port component=aaa without_buf=yes />			(Depends on simulator)	
	<pkg type=short/>					
	<pkg type=package/>					
	<pkg type=pin/>					
	<pkg type=package_model/>					
	<interconnect name=xxx/>					

<pkg/> and <interconnect/> can be written together.
 More than one <interconnect/> can be written.

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- **Conclusion & Proposal**

Conclusion & Proposal

Conclusion

- IEC 63055 / IEEE 2401 helps shorten the setup of IBIS simulation and prevent mistakes.
- IBIS 7.0 affects IEC 63055 / IEEE 2401 interface scheme
- IEC 63055/ IEEE 2041 will be updated soon for 2020 version
 - This time, there is possibility to implement the additional option to cooperate with IBIS 7.0. (this will be discussed in JEITA.)

Proposal

- For future, establish Joint work for harmonization with latest IBIS and IEEE 2401.
 - To join the web meeting or to hold the meeting with IBIS summit.
- IEEE 2401-2020 revision work – join P2401 working group if you are IEEE-SA member

Thank you!

Reference IEEE P2401

project 2013 <http://grouper.ieee.org/groups/2401/>

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P2401 WG Home Page

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WG Policies and Procedures

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Working Group for Standard Format for LSI-Package-Board Interoperable Design (C/DA/LPB)

This project is sponsored by the IEEE Computer Society/Design Automation (C/DA).

Title: Standard Format for LSI-Package-Board Interoperable Design

Scope: This standard defines a common interoperable format used for the design of (a) Large Scale Integrated (LSI) circuits, (b) Packages for such LSI circuits and (c) Printed Circuit Boards on which the packaged LSI circuits are interconnected. Collectively such designs are referred to as "LSI-Package-Board" designs. The format provides a common way to specify information/data about the project management, net lists, components, design rules, and geometries used in LSI-Package-Board designs.

Purpose: The general purpose of this standard is to develop a common format that LSI-Package-Board design tools can use to exchange information/data seamlessly, as opposed to having to work with multiple different input and output formats.

Need for the Project: Because techniques for the design of LSI circuits, packages and printed circuit boards evolved separately, the software used for such designs typically employ different formats even when accessing identical information and data. The use of these differing formats presents a barrier to the natural information flow between software tools used for LSI-Package-Board design. The common format to be standardized will eliminate this barrier, and achieve seamless information/data exchange between LSI-Package-Board software tools.

For more information, view the approved [PAR](#).

WG Officers

Chair Yoshinori Fukuba	Vice Chair Yukio Masuko	Secretary Genichi Tanaka	IEEE-SA Liaison Jonathan Goldberg
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(Last modified 03/19/2014 Goldberg)



IEC 63055/
IEEE 2401-2015

project 2017  IEEE 2401-2020 Approved PAR,
expected IEEE board committee approval by Mar.2018