LPB-SC MDL-WG
インダクタンス考慮設計手法TG
FY17 Annual Report

半導体&システム設計技術委員会

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インダクタンス考慮設計手法検討TG

- **ゴール(今年度)**
  - インダクタンス考慮の最先端デザインにおける必要性技術レポート
    - JEITA標準化を見据え論文提出を行う予定.
- **実施内容**
  - 文献、過去study調査
    - 現調査不足部分
  - インダクタンスによる影響度(電力/速度)調査
    - 先端デザインを想定
  - 現設計フローでの問題点の明確化
- **活動期間**
  - **2016/7/B → 2017/12/E (去年からの継続)**
- **リーダー**
  - ソニー)長谷川
- **メンバー**
  - ルネサス)坂田さん

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TG開催と参加人数

- 下記の日程で計6回開催した

#1 4/21 銀座 (リコー)	#2 5/23 海老名 (リコー)	#3 6/15 銀座 (リコー)	#4 7/21 銀座 (リコー)	#5 8/21 銀座 (リコー)	#6 10/27 銀座 (リコー)
3名	2名	3名	3名	3名	3名

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インダクタンス考慮設計手法検討TG

- 背景
  - LSIの高速化に伴い、クロック幹線等に対するインダクタンス考慮が必要になってきている。近年、これに対応してクロック配線等に特化して自己インダクタンス抽出を標榜するツールも現れている。しかしながら、既報の論文には、オンチップの高速配線には自己インダクタンスの考慮だけでは不十分で、相互インダクタンスの考慮が必要という調査結果が示されている。現在、オンチップのタイミング検証、およびノイズ解析に供するパワーモデリングにおいては一般に相互インダクタンス成分は考慮されていない。

- 検討内容
  - 既報の論文では、相互インダクタンス考慮有無での遅延およびパワー見積もりの誤差が示されているが、オンチップの配線構造パラメータに関して相互インダクタンスのモデリングが困難、との理由で誤差の予測式を示すには至っていない。インダクタンスTGでは、相互インダクタンスを解析式で表現するモデルを利用し、誤差の予測式を提案。それにより、自己インダクタンスまでの考慮で閉じるための設計制約、あるいは相互インダクタンスを考慮するべき配線のスクリーニング（選別）手法の標準化に繋げる。

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論文投稿先について

- 投稿先
  - 時期、費用、本投稿目的からELEX + SASIMI投稿が適切と判断
- ELEXとは
  - IEICE Electornics Express
  - 電子情報通信学会の電子ジャーナル
  - 対象はエレクトロニクス全般 (査読あり)
- SASIMIとは
  - Workshop on Synthesis And System Integration of Mixed Information technologies
  - 日本と台湾で開催されている国際学会。
  - システム、協調設計、アナログ関係が主

上程：論文投稿

- ご審議頂きたい内容
  - LPB-SC MDL-WGにおける「インダクタンス考慮設計標準化TG活動」成果をELEXとSASIMI国際学会に論文投稿する。
- 投稿内容
  - LSI設計におけるMutual Inductance考慮の必要性を述べる。
    - Mutual Inductanceを考慮しないと最先端LSI設計において5%程度の遅延値のずれが発生し、既存の設計手法では遅延値保障をすることができず、LSIを動作させられないことを立証、Mutual Inductanceを考慮した設計の標準化の必要性を述べる。
- 投稿目的
  - 人材育成
    - 学会発表経験のないメンバーが本経験をすることで視野を広げ、得られた知見を今後の活動に活かす。
  - プレゼンスの向上
    - 本委員会のプレゼンスを向上し、参加各社を広げやすくする。
  - JEITA活動の意義達成
    - 電子情報技術産業の総合的な発展に資し、わが国経済の発展と文化の興隆に寄与するため。

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上程：論文投稿：ELEX + SASIMIを選んだ理由

	ASP-DAC	ICCAD	ELEX	SASIMI	ELEX+SASIMI
概要	国際学会	国際学会	レター誌	国際学会	左記参照
内容	EDA技術、Method全般	EDA技術、Method全般	エレクトロニクス全般	EDA技術、Method全般	左記参照
サイト	韓国	アメリカ(CA)	-	日本(松江)	左記参照
申込締切	7/7	4/17	-	10/26	左記参照
開催	'19/1/M	'18/11/M	いつでも	'18/3/M	左記参照
時期	×:FY18発表になる。	×: FY18発表になる。	○:いつでもOK	○:FY17発表可	○: FY17発表可
費用	○: 約20万	△: 約30万	○:5万4千円	○:約12万	○: 約18万
人材育成	○	○	△:発表ではないため	○	○
プレゼンス	○	○	○	△:ローカルサイトでの公開のため	○: レター誌 & 国際学会発表
JEITA活動意義	○	○	○	○	○:レター誌 & 国際学会発表

・時期と本投稿目的から"ELEX + SASIMI発表"が最適と判断した。

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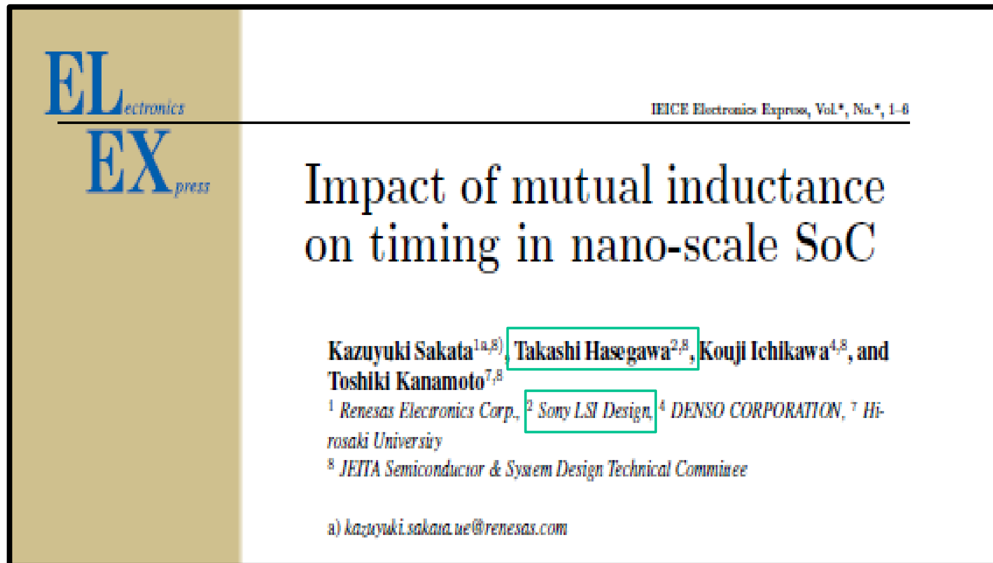
投稿概要


IEICE Electronics Express, Vol.*, No.*, 1-8

Impact of mutual inductance on timing in nano-scale SoC

Kazuyuki Sakata[1a,8], Takashi Hasegawa[2,8], Kouji Ichikawa[4,8], and Toshiki Kanamoto[7,8]
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Prediction of the impact of mutual inductance on timing towards nano-scale SoC

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- 発表内容
  - 最先端プロセスでのMutual Inductanceの考慮必要性を提案.
  - RLC ModelとRLCM Modelを比較し、5%程度の遅延値のずれが発生することを立証
  - 物理的条件からのスクリーニング手法を提案し、Mutual Inductanceを考慮したLSIモデリングの標準化の必要性を述べている。

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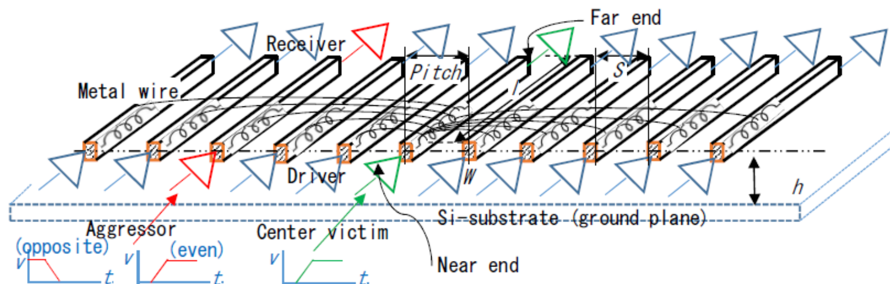
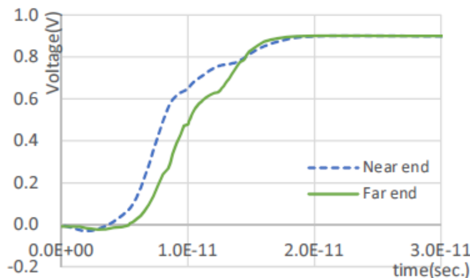
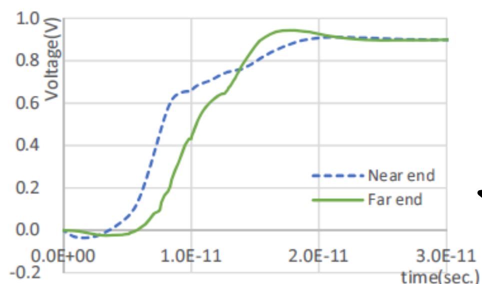
投稿概要



Simulation Model.
Spacing等をparam.として
RLC/RLCMモデルで比較

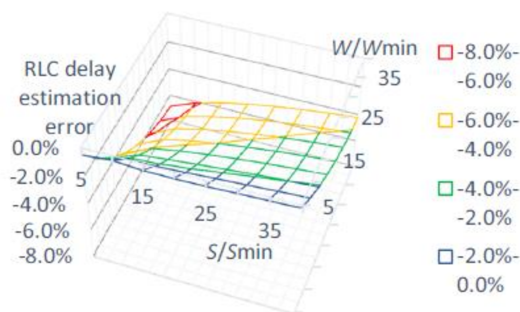


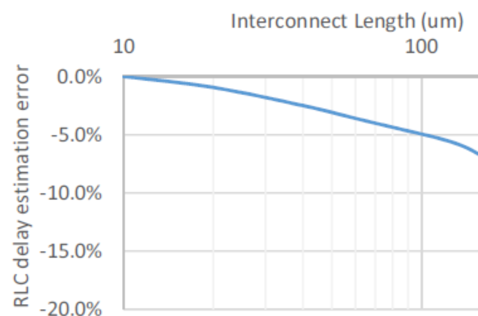
(a) RLC



(b) RLCM

RLC vs RLCMで波形の比較
Mutualを考慮することで反射が
強く見えている.





Spacingが5x spacing以下
配線幅が5x以上
配線長が100um以上
で顕著にMutual L効果が見える

Mutual Inductance考慮の必要性及びスクリーニング方法の提案を行った

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ELEX 投稿論文 1/2

ELectronics EXpress

Impact of mutual inductance on timing in nano-scale SoC

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[1] *Renesas Electronics Corp.*, [2] *Sony LSI Design*, [4] *DENSO CORPORATION*, [7] *Hirosaki University*

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Abstract: This paper investigates the impact of mutual inductance (M) on interconnect signal delay estimation according to resistance (R), inductance(L), and capacitance(C) in nano-scale system on a chip (SoC), suggesting a method to predict and suppress the impact. The proposed methodology first calculates the difference in delay between RLC and $RLMC$ wire models for a set of parameter variations, then builds response surface functions (RSF) using physical parameters including wire width and spacing. The proposed method contributes to the following actions.

1) Describe design rules to avoid mutual inductance effects.

2) Select wires which require $RLMC$ models for delay estimation

3) Correct the estimated delay when using an RLC model.

As an example, situations to limit the mutual inductance effect is shown as to a 14nm technology node.

Keywords: On chip inductance, Mutual, Screening, Delay, Timing analysis, Nano-scale, System on a chip

Classification: Electron devices, Integrated circuits, and systems

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1 Introduction

Impacts of on-chip inductance on signal propagation delay have been discussed [1]-[5] for 1 GHz or higher clock frequencies. The articles [1][2] revealed effects of on-chip self-inductance and then proposed methods for screening interconnects which should be treated as RLC models[6][7], rather than the conventional RC expressions[8]. As for the recent System-on-a-Chip (SoC) applications including 4K8K HDTV processing[9], processor cores need more speed to complete the required operations. Towards further high clock frequencies, the articles [3][5] pointed out necessity of taking into consideration the inductive coupling effects in timing analysis. In order to reappear the inductive coupling effects, we have to extract the mutual-inductance (M) in addition to the loop self-inductance (L)[10][11]. However, the existing papers have not explicitly suggested screening

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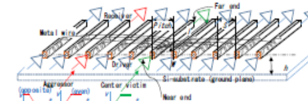

Fig. 1. Interconnect structure for screening the mutual inductance effect.

methods of on-chip mutual-inductance effects, which predict physical dimensions of interconnects to require $RLMC$ models.

This paper proposes a method to screen the mutual inductance effects on timing in terms of physical dimensions including wire width, spacing, and distance from the aggressor. It reveals layout pattern dependence of the RLC delay estimation error. Using the proposed method, we can minimize signal delay estimation errors associate with the inductive coupling.

2 Screening method of the impact of mutual inductance on timing

The overall flow consists of the following two steps.

1. Estimation of difference in signal propagation delay between wire models with and without mutual inductance (M).

2. Generation of RSF to predict the delay difference between RLMC and RLC models using physical dimension for mutual inductance impact evaluation along with precise timing analysis.

2.1 Estimation of difference in signal propagation delays

Three dimensional interconnect structures under test have cross-sectional dimensions including metal and dielectric thickness defined by the wafer process technologies. Conversely, horizontal dimensions such as width, spacing, and length of wires can be managed by designers. The horizontal dimension parameters are treated as variables. Figure 1 shows the interconnect structure. We assume regular meshes of ground grids that provides the return current. Here, all neighbors are considered as candidates of the current return path during RLC extraction with the lumped self-inductance L. On the other hand, selection of the current return path affects inductive coupling effects between the objective (victim) and the aggressor wires. To avoid excessive pessimism, the substrate plane is treated as the current return path when extracting $RLMC$. The extracted RLC and $RLMC$ form ladders so that the unit length is sufficiently small compared to the wave length derived by the significant frequency f_s [2][5]. It is expressed as the function of the signal rising time t_r and the signal falling time (Eq.(1)). The driver size is determined so that the transition at the receiver becomes t_r and t_f.

$$f_s = \frac{0.35}{t_r(t_f)}. \tag{1}$$

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ELEX 投稿論文 2/2

Table I. Predictor variables x_i to predict the difference between RLMC and RLC delays.

Variable	Explanation
S_{min}/S	Reciprocal of wire spacing normalized by the minimum.
W/W_{min}	Wire width normalized by the minimum.
l/l_{min}	Wire length normalized by the minimum.
D_{min}/D	Reciprocal of distance from the aggressor norm. by the pitch.

Table II. Interconnect parameter and constant for 14nm node.

Parameter, Constant	Unit	Variation
Relative dielectric constant	-	2.375
Wire sheet resistance	$\Omega/\square$	5.08
Wire thickness t	nm	89
Wire height h	nm	1015.8
Wire spacing S	$S_{min} = 38nm$	$\times5, \times10, \times20, \times40, \times80$
Wire width W	$W_{min} = 38nm$	$\times5, \times10, \times20, \times40, \times80$
Wire length l	$l_{min} = 10\mu m$	$\times1, \times2, \times4, \times8, \times16$
Distance from aggressor D	$Pitch = W + S$	$\times1, \times2, \times3$

2.2 Response surface function generation

After differences between RLC and RLMC delays are estimated for the parameter variation, the screening equations are built using response surface methods (RSM)[12]. We build response surface functions (RSF) expressed as Eq.(2), based on the physical dimension parameters.

$$RSF = f(x_1, x_2, \cdots, x_i, \cdots, x_n) + \epsilon \tag{2}$$

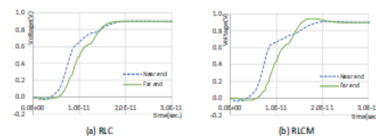
In Eq.(2), x_i denotes predictor variables which predicts the difference between RLMC and RLC delays, and ϵ expresses residual error in the prediction. In detail, referring the amount of mutual inductance[10][11] as well as the relative ratio of reactance[13], we define the RSF as the fourth order polynomial functions of the predictor variables shown in Table I.

It contributes to estimate impact of the mutual inductance in floor-planning, or physical design phases.

3 Quantitative evaluation of the screening method in a 14nm FinFET process

Based on the parameters in International Technology Roadmap for Semiconductors (ITRS) [14] along with Predictive Technology Model (PTM)[15], the interconnect structure with buffers and receivers for high-performance SoC are defined as shown in TableII.

We apply the proposed method to the 14 nm technology node to evaluate prediction of the mutual inductance effects. Size of the drivers and the receivers is $\times64$ of the unit size[16] so that t_r and t_f becomes 10ps., where the operating frequency is targeted at 10GHz and the significant frequency f_s is 35GHz. The corresponding wavelength is 3.6mm. According to a preliminary experiment, domain of the

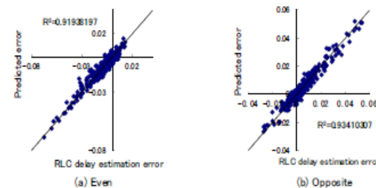


(a) RLC (b) RLCM

Fig. 2. Simulated signal propagation with and without mutual inductance.

horizontal dimension parameters are decided so that the maximum relative delay difference exceeds 5%. Since the wire length is below a quarter of the wavelength, we apply a FEM based 2.5D field solver[17]. Figure 2 compares RLC and RLMC waveforms when both the victim and the aggressor signals transition in the same direction (even). We separate the opposite transition from the even case because the mutual inductance effects act reversely for these two cases. Here, the self inductance varies from 0.47nH/mm to 0.96nH/mm, whereas the mutual inductance between the adjacent interconnects varies from 0.11nH/mm to 0.52nH/mm.

Figure 3 shows the RLC delay estimation errors compared to the RLMC delays with the corresponding predictions using the RSFs. The degree of freedom

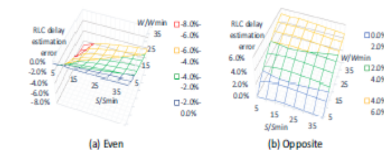


(a) Even (b) Opposite

Fig. 3. Prediction accuracy of the delay estimation without mutual inductance.

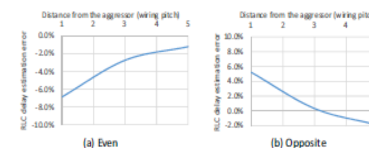
adjusted coefficient of determination (R^2) exceeds 0.9, which indicates that the prediction has good fit[12].

Figure 4 depicts wire width and spacing dependence of the mutual inductance effect. The wire length is fixed to $160\mu m$ here. We can read that the impact of the mutual inductance increases with the wire width. It exceeds 5% when the wire width is larger than 35 times of the minimum width. Contrary, wire spacing mitigates the impacts. Even when the wire width is larger than 35 times, we can suppress the impact within 5% by making the wire spacing wider than 20 times of the minimum spacing. Figure 5 shows that the distance from the aggressor wire also reduces the impacts. In terms of length, longer wires result in larger impacts as shown in Fig.



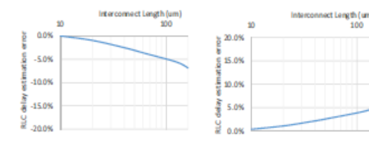
(a) Even (b) Opposite

Fig. 4. Impact dependence on wire width and spacing.



(a) Even (b) Opposite

Fig. 5. Impact dependence on distance from the aggressor.



(a) Even (b) Opposite

Fig. 6. Impact dependence on wire length.

6. In this case, the RLC modeled delay cause 5% or larger errors with $100\mu m$ or longer wires.

4 Conclusion

This paper studied the impact of mutual inductance on interconnect signal delay estimation in a nano-scale system on a chip (SoC), suggesting a method to dimensionally predict and then screen the impact. The proposed methodology first calculates the delay difference between RLC and $RLMC$ wire models for a set of parameter variations, then builds RSFs using dimensional parameters including wire width and spacing. The proposed method helps to avoid mutual inductance effects by pointing out interconnects which require $RLMC$ delay models, as well as to correct the estimated delay using RLC models.

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SASIMI 投稿論文 1/1

Prediction of the impact of mutual inductance on timing towards nano-scale SoC

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Toshiki Kanamoto, Hirosaki University, JEITA Semiconductor, kana@hirosaki-u.ac.jp

Abstract— This paper suggests a method to predict the impact of mutual inductance (*M*) on interconnect signal delay estimation according to resistance (*R*), self-inductance(*L*), and capacitance(*C*) in nano-scale system on a chip (SoC). The proposed method first calculates the difference in delay between *RLC* and *RLMC* wire models for a set of parameter variations, then builds response surface functions (RSF) using physical parameters including wire width and spacing. The proposed method contributes to describe design rules to avoid mutual inductance effects.

I. Introduction

Impacts of on-chip inductance on signal propagation delay have been discussed [1]-[6] for 1 GHz or higher clock frequencies. The articles [1][2] revealed effects of on-chip self-inductance and then proposed methods for screening interconnects which should be treated as *RLC* models[7][8], rather than the conventional *RC* expressions[9]. As for the recent System-on-a-Chip (SoC) applications including 4K8K HDTV processing[10], processor cores need more speed to complete the required operations. Towards further high clock frequencies, the articles [3][4][5][6] pointed out necessity of taking into consideration the inductive coupling effects in timing analysis. In order to reappear the inductive coupling effects, we have to extract the mutual-inductance (*M*) in addition to the loop self-inductance (*L*)[11][12]. However, the existing papers have not explicitly suggested screening methods of on-chip mutual-inductance effects, which predict physical dimensions of interconnects to require *RLMC* models.

This paper proposes a method to screen the mutual inductance effects on timing in terms of physical dimensions including wire width, spacing, and distance from the aggressor. It reveals layout pattern dependence of the *RLC* delay estimation error. Using the proposed method, we can minimize signal delay estimation errors associate with the inductive coupling.

II. Screening method of the impact of mutual inductance on timing

The overall flow consists of the following two steps.

A. Estimating difference in signal propagation delay between wire models with and without mutual inductance (*M*).

B. Generating RSF to predict the delay difference between RLMC and RLC models using physical dimension for mutual inductance impact evaluation along with precise timing analysis.

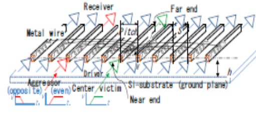


Fig. 1.: Interconnect structure for screening the mutual inductance effect.

A. Estimation of difference in signal propagation delays

Three dimensional interconnect structures under test have cross-sectional dimensions including metal and dielectric thickness defined by the wafer process technologies. Conversely, horizontal dimensions such as width, spacing, and length of wires can be managed by designers. The horizontal dimension parameters are treated as variables. Figure 1 shows the interconnect structure. We assume regular meshes of ground grids that provides the return current. Here, all neighbors are considered as candidates of the current return path during *RLC* extraction with the lumped self-inductance *L*. On the other hand, selection of the current return path affects inductive coupling effects between the objective (victim) and the aggressor wires. To avoid excessive pessimism, the substrate plane is treated as the current return path when extracting *RLMC*. The extracted *RLC* and *RLMC* form ladders so that the unit length is sufficiently small compared to the wave length derived by the significant frequency f_s [2][6]. It is expressed as the function of the signal rising time t_r and the signal falling time (Eq.(1)). The driver size is determined so that the transition at the receiver becomes t_r and t_f.

$$f_s = \frac{0.35}{t_r(t_f)} \quad (1)$$

TABLE I
: Predictor variables x_i to predict the difference between RLMC and RLC delays.

Variable	Explanation
S_{min}/S	Reciprocal of wire spacing normalized by the minimum.
W/W_{min}	Wire width normalized by the minimum.
l/l_{min}	Wire length normalized by the minimum.
D_{min}/D	Reciprocal of distance from the aggressor norm. by the pitch.

TABLE II
: Interconnect parameter and constant for 14nm node.

Parameter, Constant	Unit	Variation
Relative diel. const.	-	2.375
Wire sheet resistance	Ω/□	5.08
Wire thickness *t*	nm	89
Wire height *h*	nm	1015.8
Wire spacing *S*	$S_{min} = 190nm$	×1, 2, 4, 8, 16
Wire width *W*	$W_{min} = 190nm$	×1, 2, 4, 8, 16
Wire length *l*	$l_{min} = 10\mu m$	×1, 2, 4, 8, 16
Distance from aggressor	$Pitch = W + S$	×1, 2, 3

B. Response surface function generation

After differences between RLC and RLMC delays are estimated for the parameter variation, the screening equations are built using response surface methods (RSM)[13]. We build response surface functions (RSF) expressed as Eq.(2), based on the physical dimension parameters.

$$RSF = f(x_1, x_2, \cdots, x_i, \cdots, x_n) + \epsilon \quad (2)$$

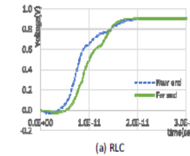
In Eq.(2), x_i denotes predictor variables which predicts the difference between RLMC and RLC delays, and ϵ expresses residual error in the prediction. In detail, referring the amount of mutual inductance[11][12] as well as the relative ratio of reactance[14], we define the RSF as the fourth order polynomial functions of the predictor variables shown in Table I.

It can contribute to estimate the inductance impact in floor-planning, or physical design phases.

III. Quantitative evaluation of the screening method in a 14nm FinFET process

Based on the parameters in International Technology Roadmap for Semiconductors (ITRS) [15] along with Predictive Technology Model (PTM)[16], the interconnect structure with buffers and receivers for high-performance SoC are defined as shown in TableII.

We apply the proposed method to the 14 nm technology node to evaluate prediction of the mutual inductance effects. Size of the drivers and the receivers is ×64 of the unit size[17] so that t_r and t_f becomes 10ps., where the operating frequency



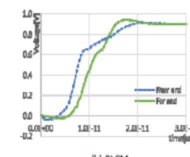
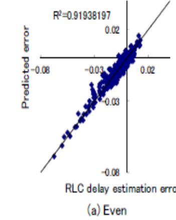


Fig. 2.: Simulated signal propagation with and without mutual inductance.

is targeted at 10GHz and the significant frequency f_s is 35GHz. The corresponding wavelength is 3.6mm. According to a preliminary experiment, domain of the horizontal dimension parameters are decided so that the maximum delay difference exceeds 3%. Since the wire length is below a quarter of the wavelength, we apply a FEM based 2.5D field solver[18]. Figure 2 compares RLC and RLMC waveforms. Figure 3 shows the RLC delay estimation errors compared to the RLMC delays with the corresponding predictions using the RSFs. The degree of freedom adjusted coefficient of determination (R^2) exceeds 0.9, which indicates that the prediction has good fit[13]. Figure 4 shows an impact dependency on distance from the aggressor.

IV. Conclusion

This paper suggested a methodology to precisely predict and then screen the impact of mutual inductance on interconnect signal delay estimation in a nano-scale system on a chip (SoC). The proposed methodology first calculates the delay difference between *RLC* and *RLMC* wire models for a set of parameter variations, then builds RSFs using physical parameters including wire width and spacing. The proposed methodology can help to define design rules for avoiding mutual inductance effects as well as to point out wires that require *RLMC* delay calculation.



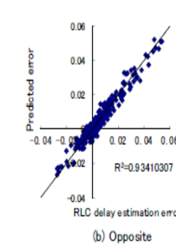
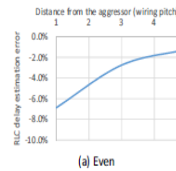


Fig. 3.: Prediction accuracy of the delay estimation without mutual inductance.



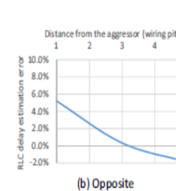


Fig. 4.: Predicted impact dependency on distance from the aggressor.

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