IEEE Design Automation Standards Committee (DASC) Report to IEC TC91 WG13

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Chair, IEEE DASC

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Introduction to the DASC

- One of the oldest Standards Committees
  - Founded in 1987
- DASC Scope
  - The IEEE DASC is responsible for the standardization of Design Automation and related Semiconductor-related Intellectual Property (IP) standards in the IEEE. The DASC is focused on language-based design, modeling, integration, and verification standards. This includes standards for timing, synthesis, algorithms, low power, IP reuse, IP encryption, and test.
- 37 members from 17 companies in the Electronics industry represented
- Meets the first Thursday of each month online and once per year face-to-face
  - Met in person at DVCon U.S. 2023 in March 2023
- Updated Policies and Procedures in 2022

Join IEEE DASC

- DASC Membership is *Individual-based*
  - New P&Ps removed *Entity* level membership

- Join email reflector
  - Send email to ListServe@ieee.org
  - Include in the Body of the email:
    - "Subscribe STDS-DASC FirstName LastName"
  - Scan the QR Code to the right

- Membership is free

- Voting rights require
  - Attend 3 of 4 meetings
  - Pay the annual meeting fee ($40)

DASC and Other Standards Groups

- Accellera Systems Initiative
  - "[Get Design Automation Standards](#)" facilitated by Accellera
  - Accellera work continues to transfer into the DASC
- Si2
  - Originates contributions to P1801, P2416, and P2401
- JEITA
  - Representatives join DASC F2F meeting at DVCon and DAC
  - Tradition of November plenary meeting in Japan
- IEEE Standards Committee
  - Functional Safety Standards Committee (FSSC)
  - Council on EDA Standards Committee (CEDA SC)

DASC & CEDA SC Leadership

- Council on EDA (CEDA) Standards Committee
  - CEDA SC leadership and DASC leadership the same to launch CEDA SC

Position	DASC	CEDA SC
Chair	Dennis Brophy	Aparna Dey
Vice-Chair	Yatin Trivedi	Dennis Brophy
Secretary/Treasure	Aparna Dey	Yatin Trivedi

- CEDA SC Focus
  - Open Source
  - Standards Projects needing more academic input

DASC Work Program

Project Number	Project Type	Project Title	Project Status
P1076	Revision	Standard for VHDL Language Reference Manual	Draft Development
1076.1	Revision	Standard VHDL Analog and Mixed-Signal Extensions	Completed
1481	Revision	Standard for Integrated Circuit (IC) Open Library Architecture	Completed
1647	Revision	Standard for the Functional Verification Language e	Completed
P1666	Revision	Standard for Standard SystemC Language Reference Manual	RevCom Agenda(15 May 2023)
1666.1	New	SystemC Analog/Mixed-Signal (AMS) extensions Language Reference Manual	Completed
1685	Revision	Standard for IP-XACT, Standard Structure for Packaging, Integrating, and Reusing IP within Tool Flows	Completed
P1735	Revision	Recommended Practice for Encryption and Management of Electronic Design Intellectual Property (IP)	RevCom Agenda(28 Jun 2023)
P1800	Revision	Standard for SystemVerilog--Unified Hardware Design, Specification, and Verification Language	SA Ballot: Comment Resolution
1800.2	Revision	Standard for Universal Verification Methodology Language Reference Manual	Completed
P1801	Revision	Standard for Design and Verification of Low Power, Energy Aware Electronic Systems	SA Ballot: Invitation
2401	Revision	Standard Format for LSI-Package-Board Interoperable Design	Completed
P2416	Revision	Standard for Power Modeling to Enable System-Level Analysis	Draft Development
2804	New	Software-Hardware Interface for Multi-Many-Core	Completed
P3164	New	Standard for Security Annotation for Electronic Design Integration	Draft Development

DASC Active Projects

Project Number	Project Title	Project Type	Committee	Approval Date	Expiration Date
P1076	Standard for VHDL Language Reference Manual	Revision	C/DA/P1076	08 Dec 2021	31 Dec 2025
P1666	Standard for Standard SystemC Language Reference Manual	Revision	C/DA/SystemC	14 May 2018	31 Dec 2023
P1735	Recommended Practice for Encryption and Management of Electronic Design Intellectual Property (IP)	Revision	C/DA/IP Encryption	15 Feb 2018	31 Dec 2024
P1800	Standard for SystemVerilog-- Unified Hardware Design, Specification, and Verification Language	Revision	C/DA/1800_WG	07 Nov 2019	31 Dec 2023
P1801	Standard for Design and Verification of Low Power, Energy Aware Electronic Systems	Revision	C/DA/UPF	05 Dec 2018	31 Dec 2024
P2416	Standard for Power Modeling to Enable System-Level Analysis	Revision	C/DA/System Level Power Modeling	13 Feb 2020	31 Dec 2024
P3164	Standard for Security Annotation for Electronic Design Integration	New	C/DA/SA-EDI-IND	03 Dec 2022	31 Dec 2026

DASC Co-Sponsored Standards

Project Number	Project Title	Project Type	Committee	Approval Date	Expiration Date
P2851	Standard for Functional Safety Data Format for Interoperability within the Dependability Lifecycle	New	C/FSSC/Functional Safety Format	08 Dec 2021	31 Dec 2023

Seven Standards Approved for Dual Logo

▣ IEEE 1076-2019 "IEEE Standard for VHDL Language Reference Manual" for adoption as IEC 61691-1-1 ED3

▣ IEEE 1481-2019 "IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA) for adoption as IEC 61523-1 ED3

▣ IEEE 1800.2-2020 "IEEE Standard for Universal Verification Methodology Language Reference Manual" for adoption as IEC 62530-2 ED2

▣ IEEE 1801-2018 "Design and Verification of Low-Power, Energy-Aware Electronic Systems" for adoption as IEC 61523-4 ED2

▣ IEEE 2401-2019 "IEEE Standard for Format for LSI-Package-Board Interoperable Design" for adoption as IEC 63055 ED2

▣ IEEE 2416-2019 "IEEE Standard for Power Modeling to Enable System Level Analysis" for a new publication

▣ IEEE 2804-2019 "IEEE Standard for Software-Hardware Interface for Multi-Many-Core" as a new publication

QUESTIONS?