#### LSI-Package-Board

JEITA LPB相互設計セミナー 相互設計の課題とソリューション

~なぜ我々はLPBを始めたのか?~

2012/3/14

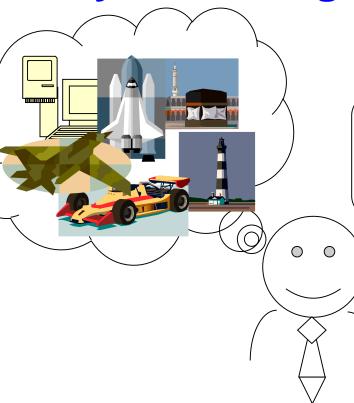
JEITA LPB相互設計ワーキンググループ

- Why we need LPB format?
- Working with LPB format.

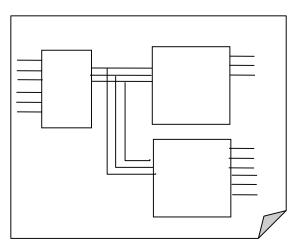




#### System designer

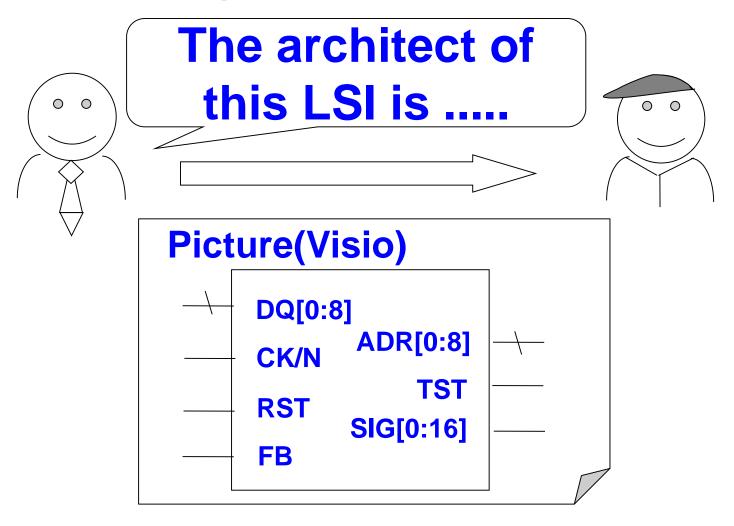


I need a new LSI for my product



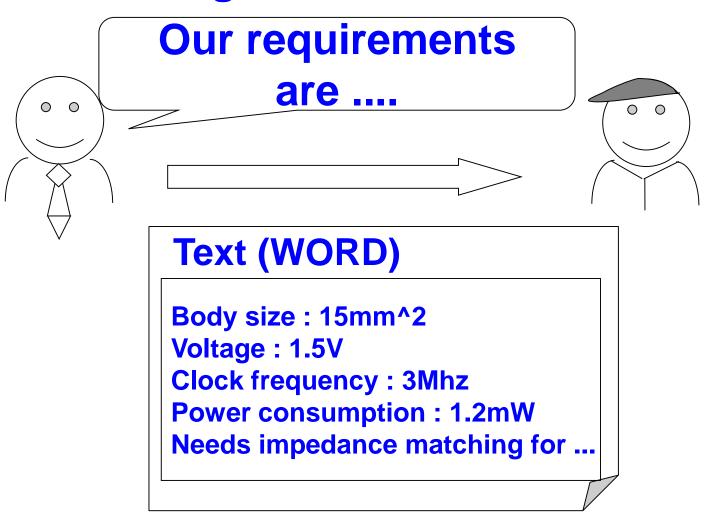
#### System designer

#### LSI designer



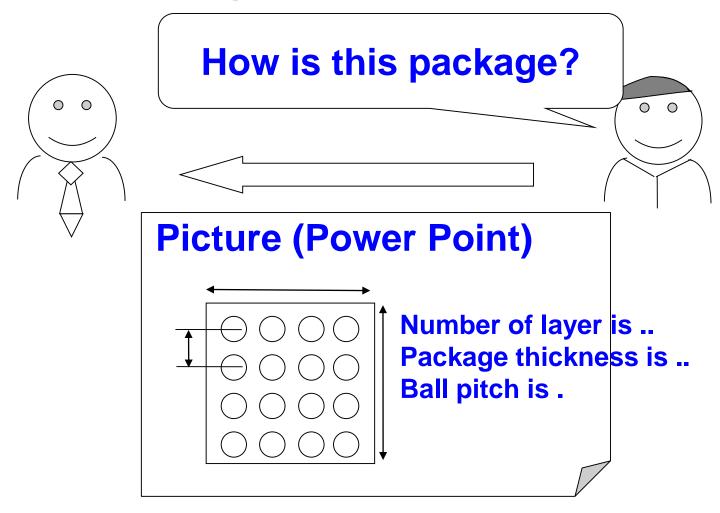
#### System designer

#### LSI designer



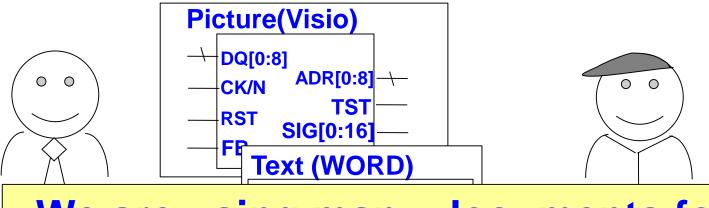
#### System designer

#### LSI designer

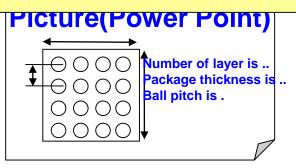


#### System designer

#### LSI designer

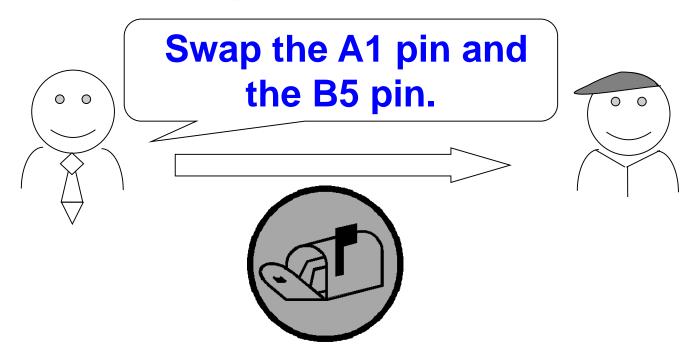


We are using many documents for the communication.



#### System designer

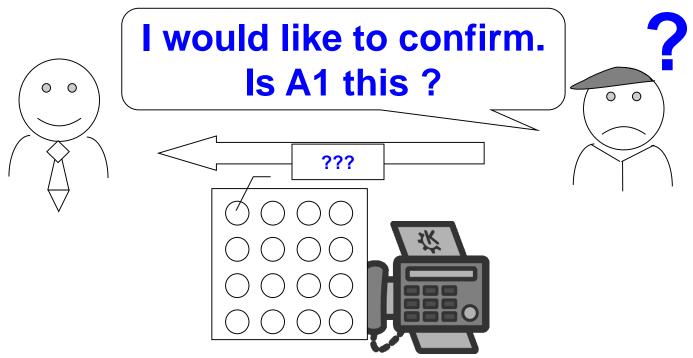
#### LSI designer



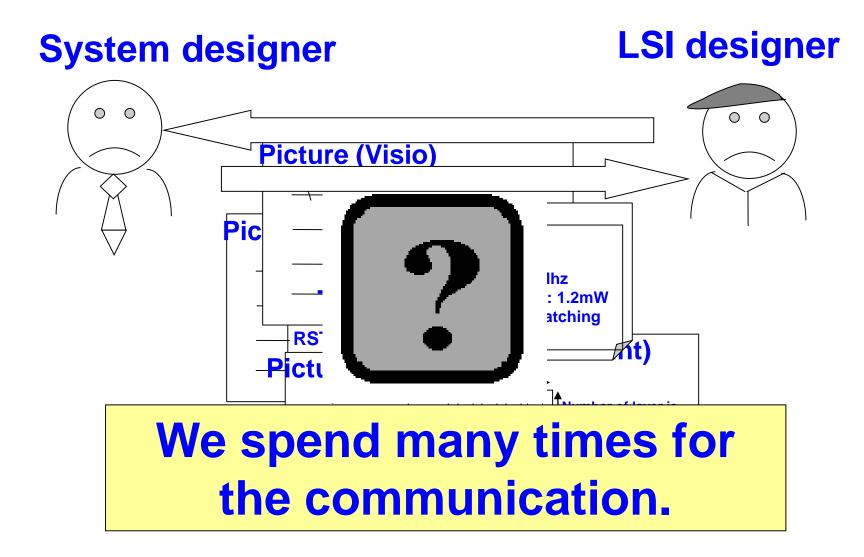
E-mail without documents maintenance.

#### System designer

#### LSI designer

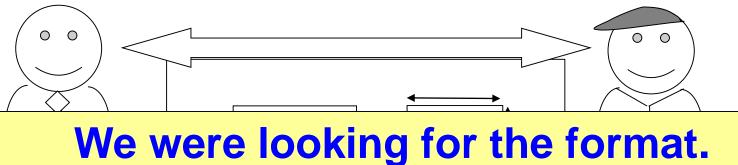


FAX without documents maintenance.



#### System designer

#### LSI designer



But we could not find it.

Body size : 15mm^2

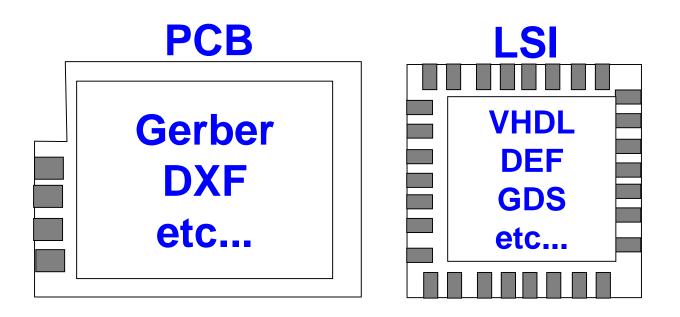
Voltage: 1.5V

Clock frequency: 3Mhz
Power consumption: 1.2mW

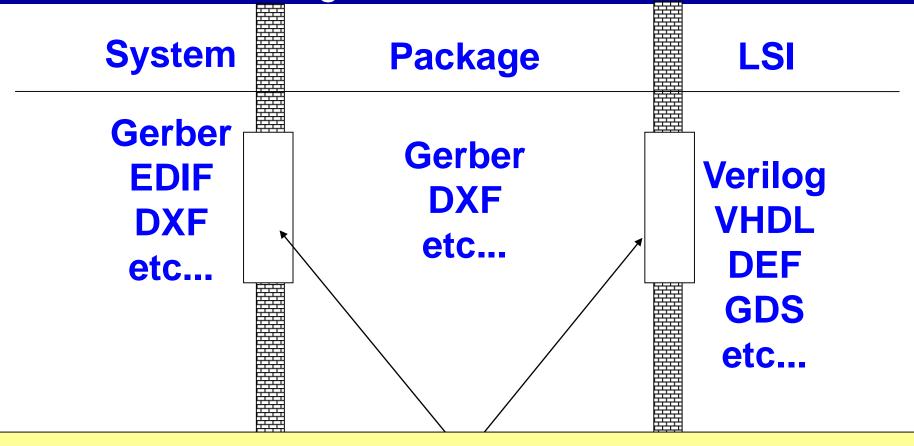
Needs impedance matching

for ...

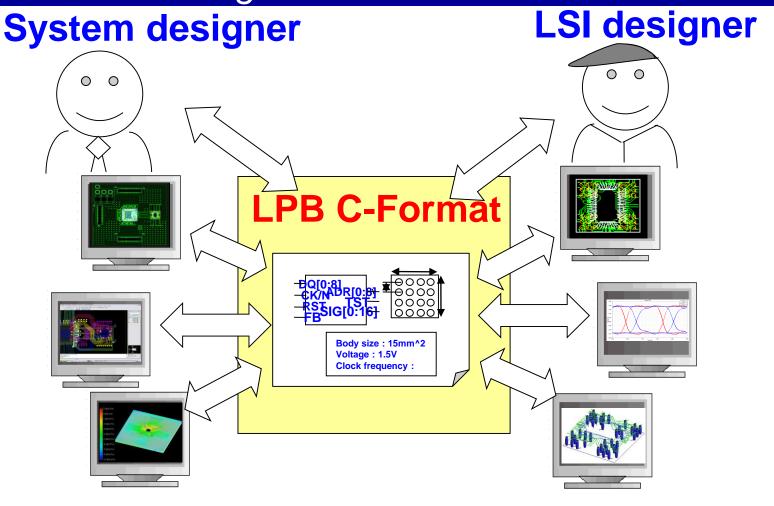
"We have to communicate with one document"



All formats are used to define the inside of object.



The something is LPB C-Format. We call the boundary as a socket.



## **LPB C-Format**

C is component or communication

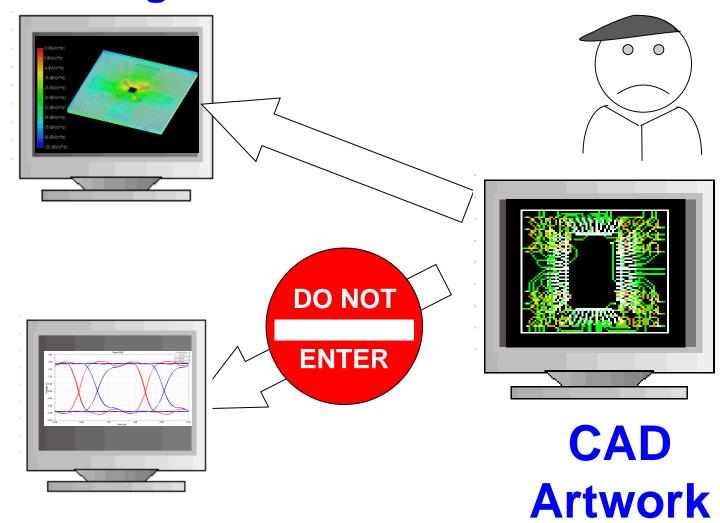
#### Why we need LPB format?

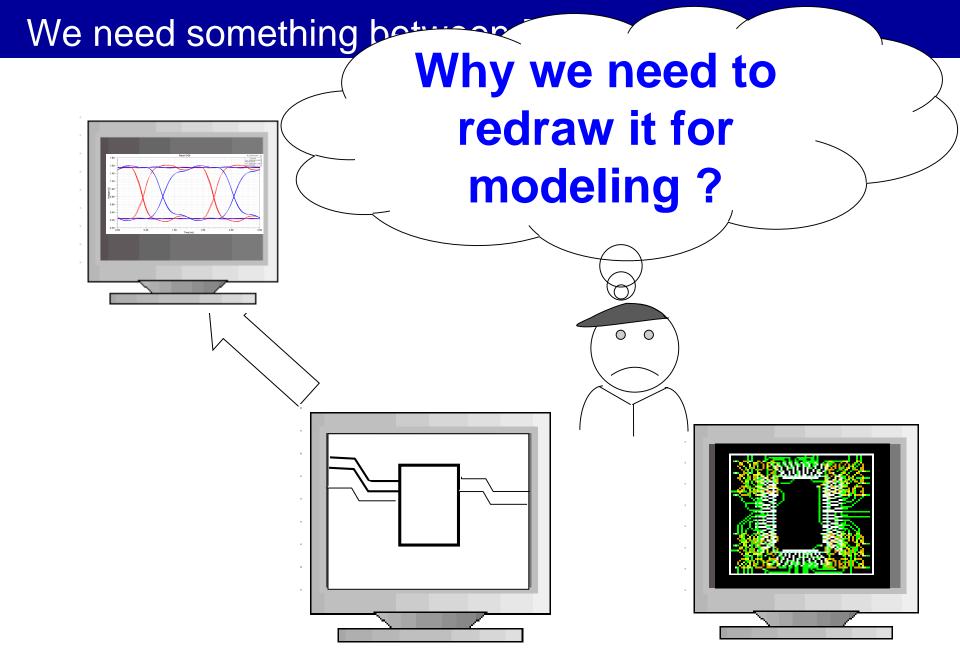
## We need a something between EDA tools.



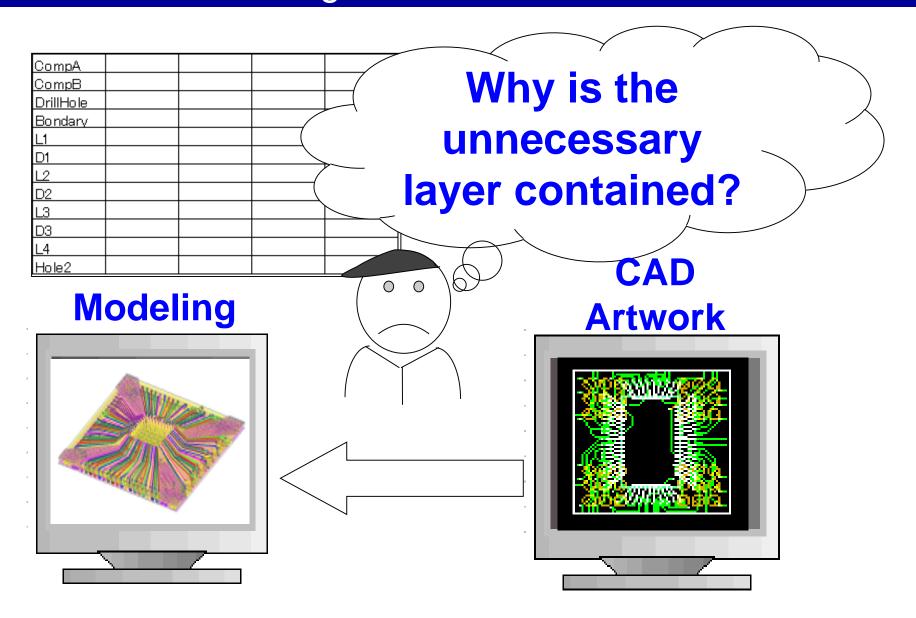
#### We need something between EDA tools.

#### Modeling

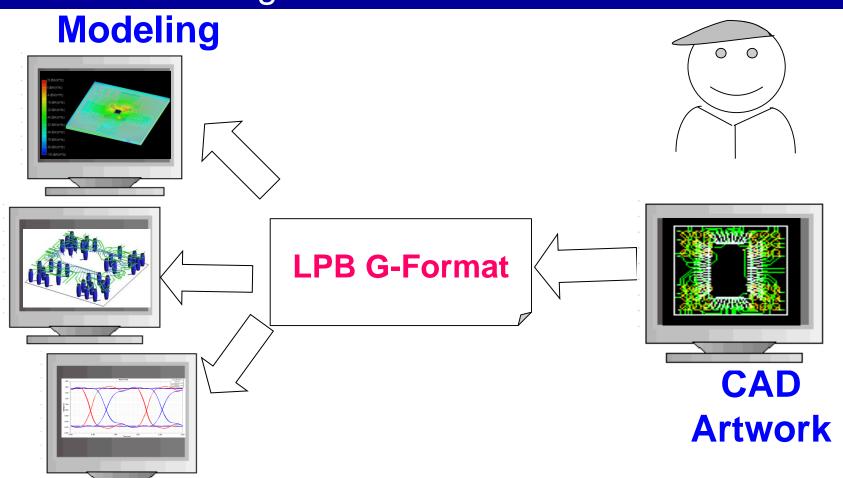




#### We need something between EDA tools.



#### We need something between EDA tools.



**LPB G-Format** 

G is geometry



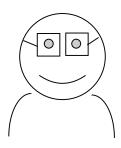
#### Package vendor

Could you send me a design rule?

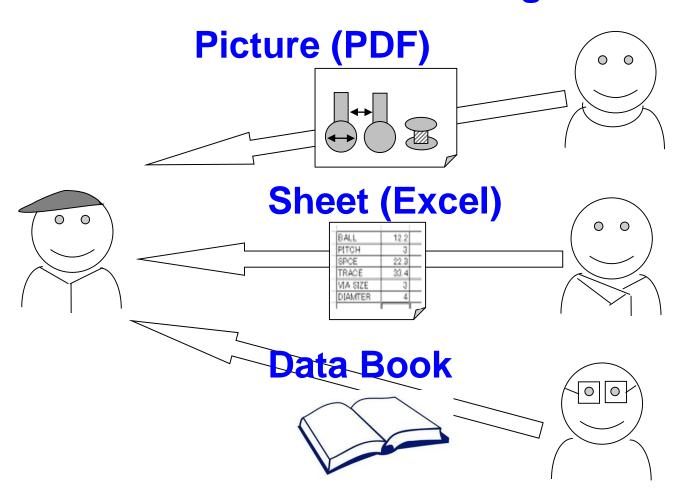
0 0





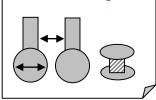


#### Package vendor



Which one is the best for my project?





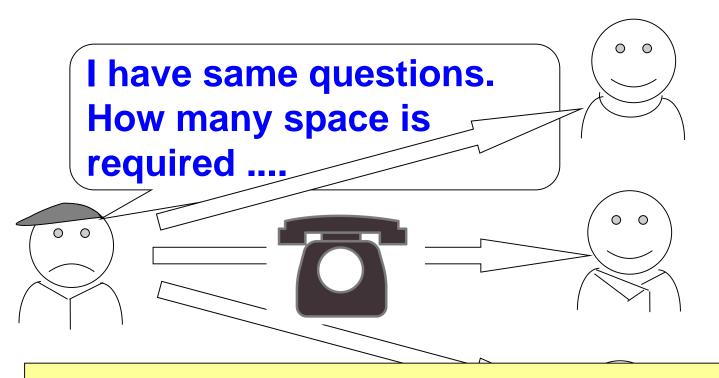
Sheet (Excel)

BALL	12.2	ı
PITCH	3	ı
SPCE	22.3	ı
TRACE	33.4	ı
VIA SIZE	3	ı
DIAMTER	4	ı
		١

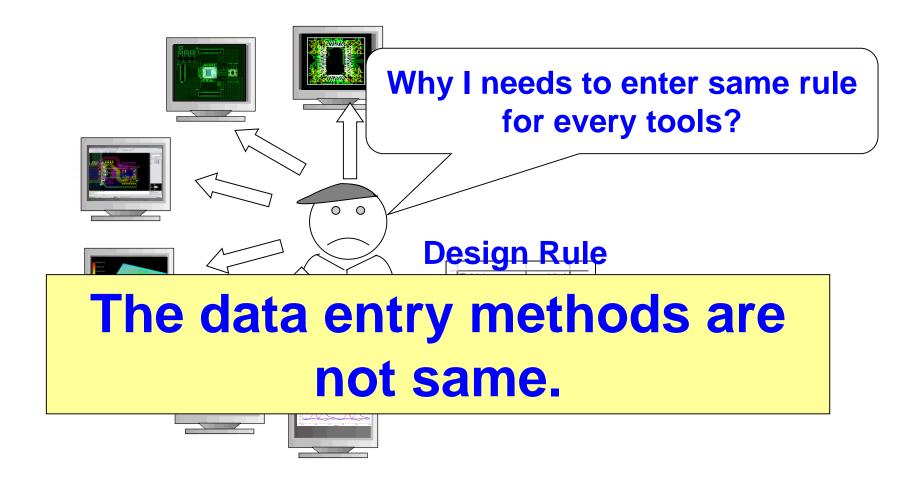
**Data Book** 

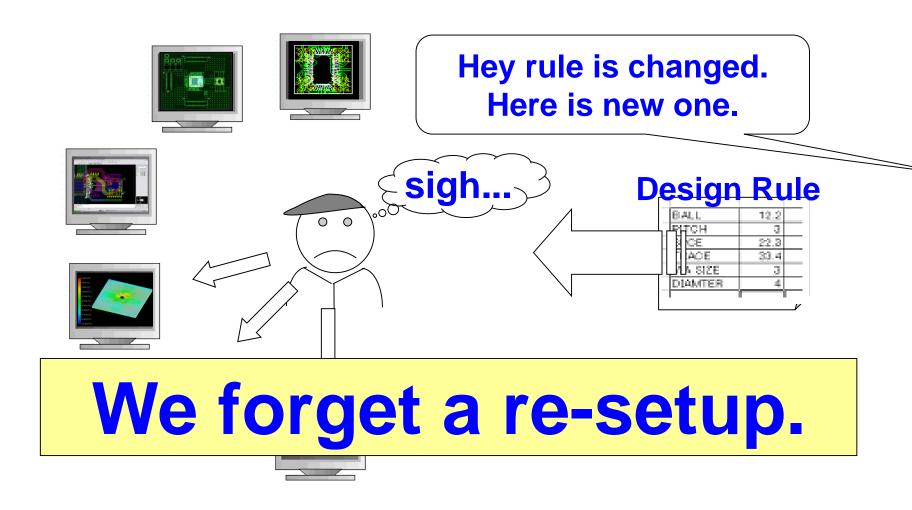


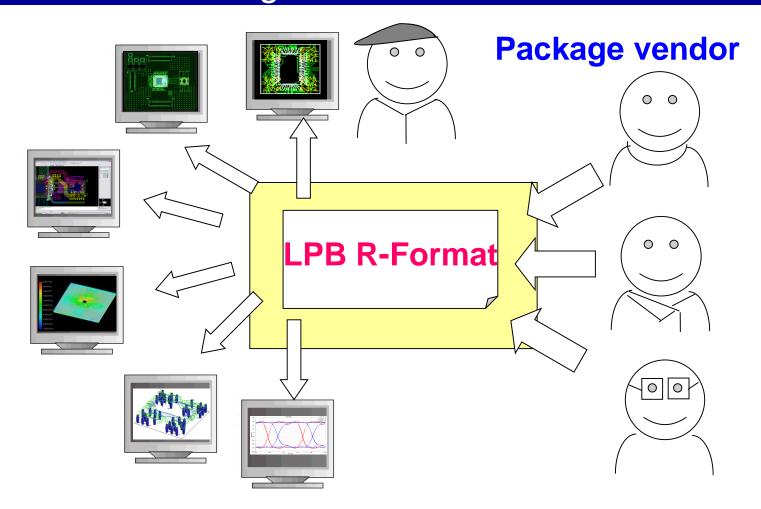
#### Package vendor



We have to spend long time to understand the design rule.







## **LPB R-Format**

R is rule

#### Why we need LPB format?

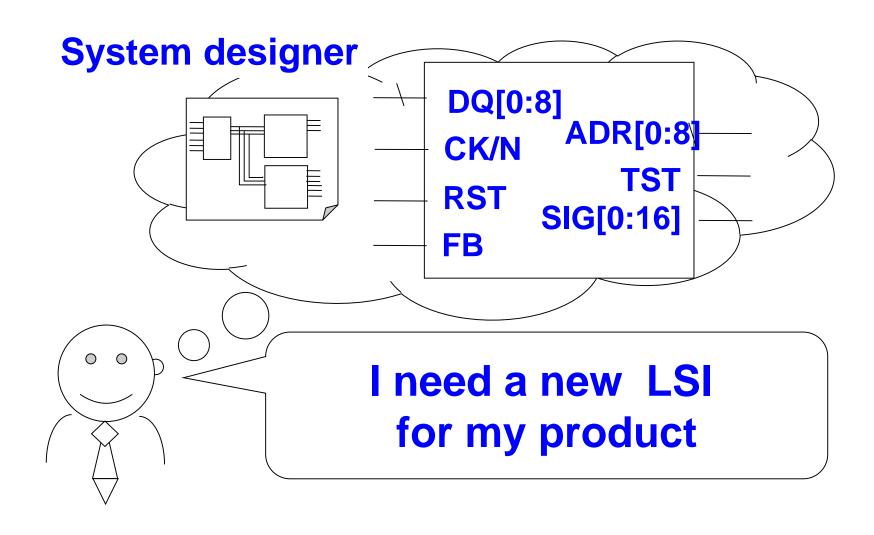
### N-Format

N is netlist.

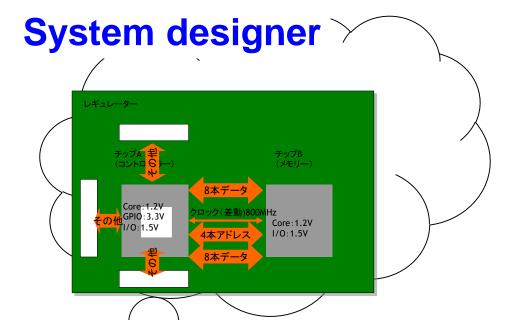
M-Format

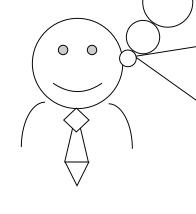
M is management.







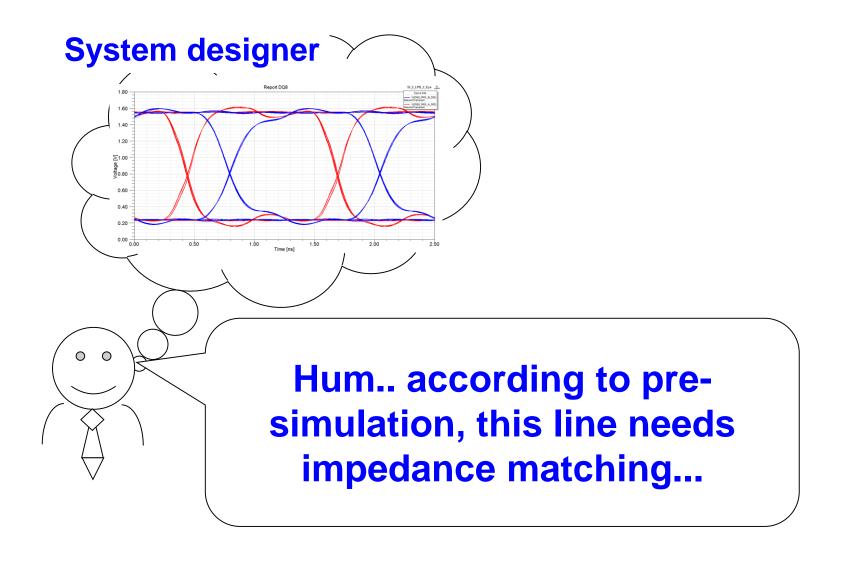




Hum.. According to this floorplan, the body size of new LSI should be ....

#### System designer

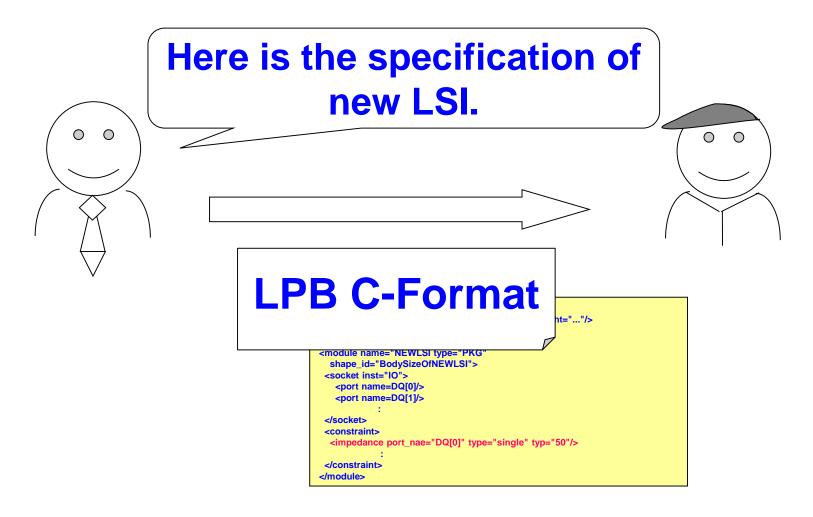
```
<shape>
 <rectangle id="BodySizeOfNEWLSI" width=".." height="..."/>
</shape>
<module name="NEWLSI type="PKG"</pre>
  shape_id="BodySizeOfNEWLSI">
 <socket inst="IO">
   <port name=DQ[0]/>
   <port name=DQ[1]/>
 </socket>
</module>
                   new LSI should be ....
```

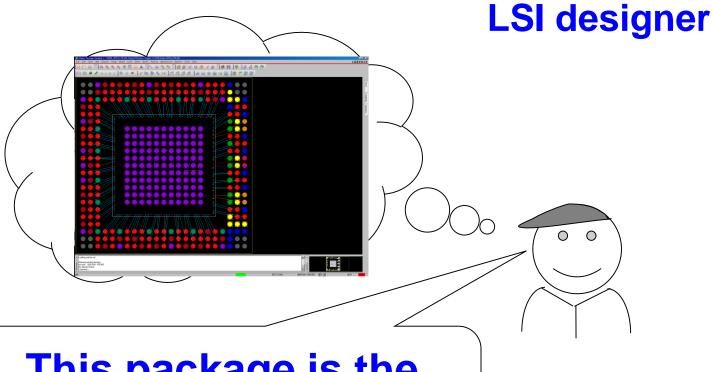


```
<shape>
 <rectangle id="BodySizeOfNEWLSI" width=".." height="..."/>
</shape>
<module name="NEWLSI type="PKG"</pre>
  shape_id="BodySizeOfNEWLSI">
 <socket inst="IO">
   <port name=DQ[0]/>
   <port name=DQ[1]/>
 </socket>
 <constraint>
  <impedance port_name="DQ[0]" type="single" typ="50"/>
 </constraint>
</module>
```

#### System designer

#### LSI designer



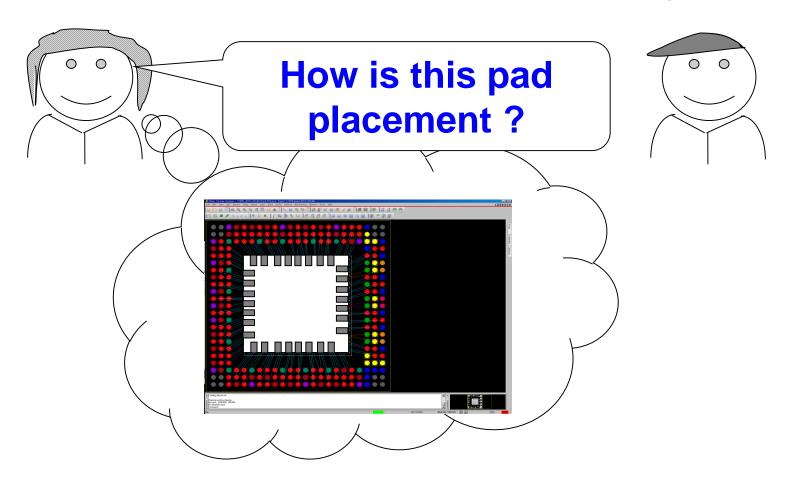


This package is the best for this project.

```
<circle id BallSize diameter="..."/>
</shape>
<padstack def>
 <padstack id="BallPad" type="BALL PAD">
   <ref_shape shape_id="BallSize" layer="BOTTOM"/>
 </padstack>
</padstack_def>
<module name="NEWLSI" type="PKG" shape_id="BodySizeOfNEWLSI">
 <socket inst="IO">
   <default>
     <port_shape padstack_id="BallPad" />
   </default>
   <port name=DQ[0]/>
   <port name=DQ[1]/>
   <port id="A1" x=".." y=".."/>
   <port id="A2" x=".." y=".."/>
 </socket>
 <constraint>
  <impedance port_nae="DQ[0]" type="single" typ="50"/>
 </constraint>
</module>
```

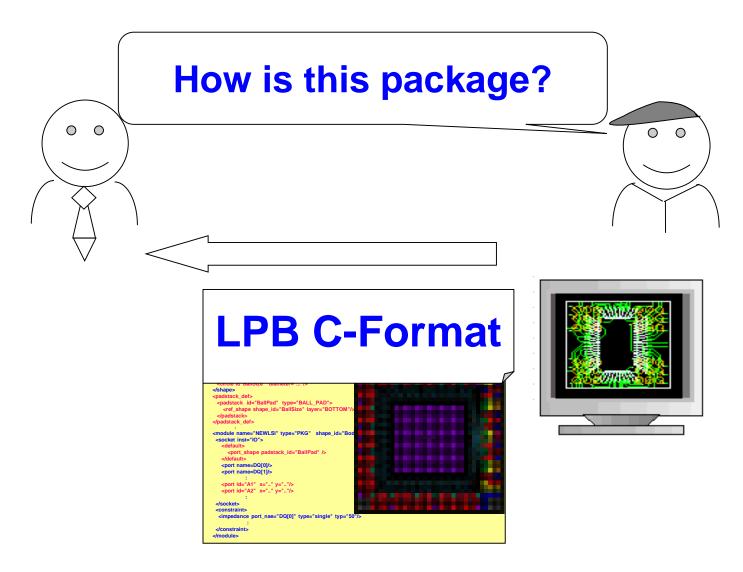
#### **Chip Layout engineer**

#### LSI designer

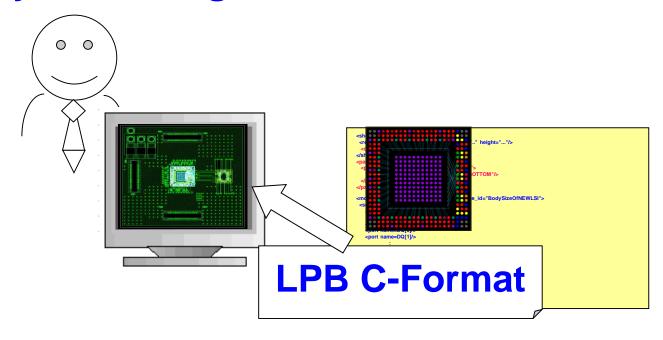


```
<shape>
</shape>
                                                    ner
<padstack_def>
</padstack_def>
<module name="NEWLSI type="LSI"</pre>
shape_id="DieSize">
 <socket inst="IO">
   <default>
     <port_shape padstack_id="Pad" />
   </default>
   <port id="P1" name="DQ_0" x=".." y=".."/>
   <port id="P2" name="DQ_1" x=".." y=".."/>
 </socket>
</module>
```

#### **System designer**

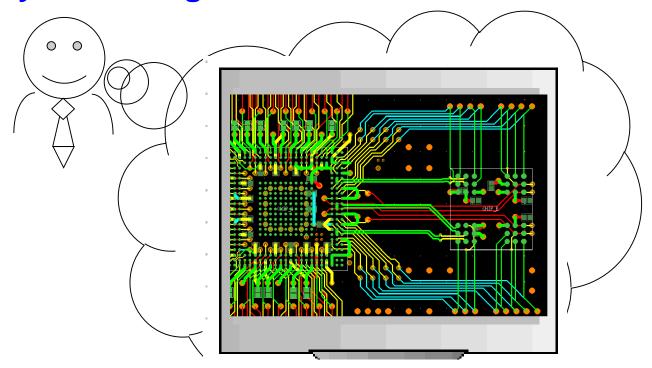


# System designer



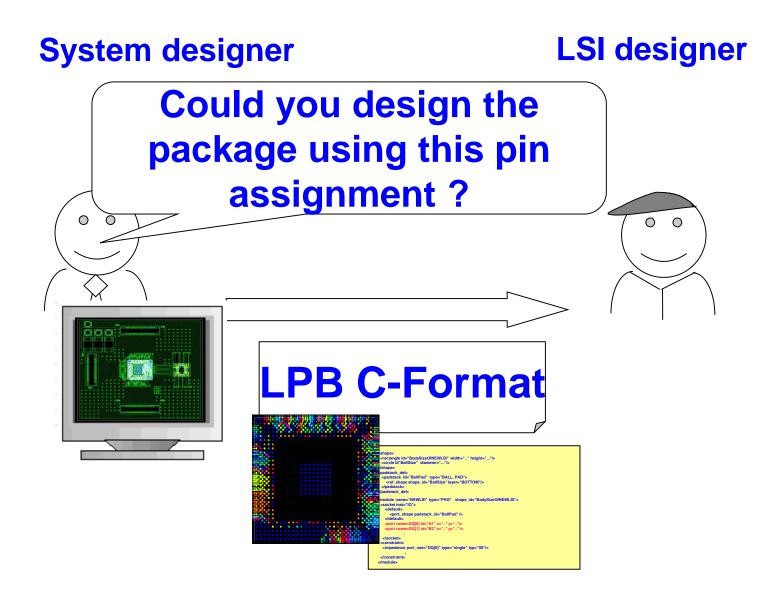
Re-build the package symbol using the C-Format.

#### **System designer**

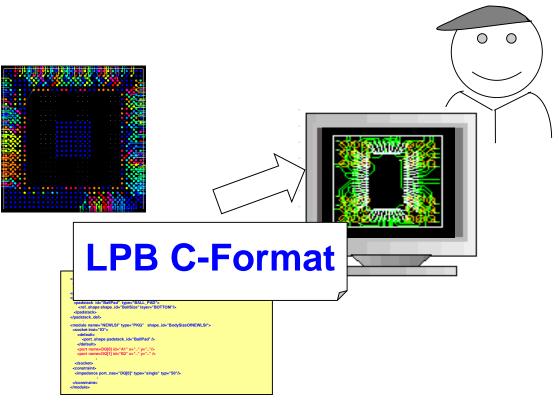


Consider the net assignment to package pin.

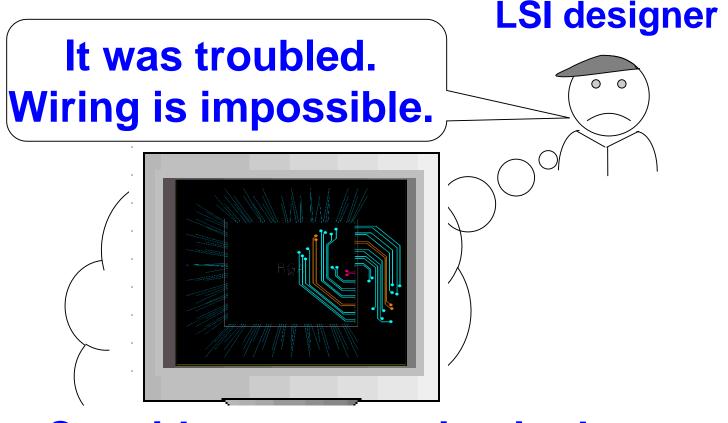
```
<rectangle id="BodySizeOfNEWLSI" width=".." height="..."/>
 <circle id"BallSize" diameter="..."/>
</shape>
<padstack_def>
 <padstack id="BallPad" type="BALL_PAD">
   <ref_shape shape_id="BallSize" layer="BOTTOM"/>
 </padstack>
</padstack_def>
<module name="NEWLSI" type="PKG"</pre>
shape_id="BodySizeOfNEWLSI">
 <socket inst="IO">
   <default>
     <port_shape padstack_id="BallPad" />
   </default>
   <port name=DQ[0] id="A1" x=".." y=".."/>
   <port name=DQ[1] id="B2" x=".." y=".." />
  </socket>
 <constraint>
  <impedance port_nae="DQ[0]" type="single" typ="50"/>
```



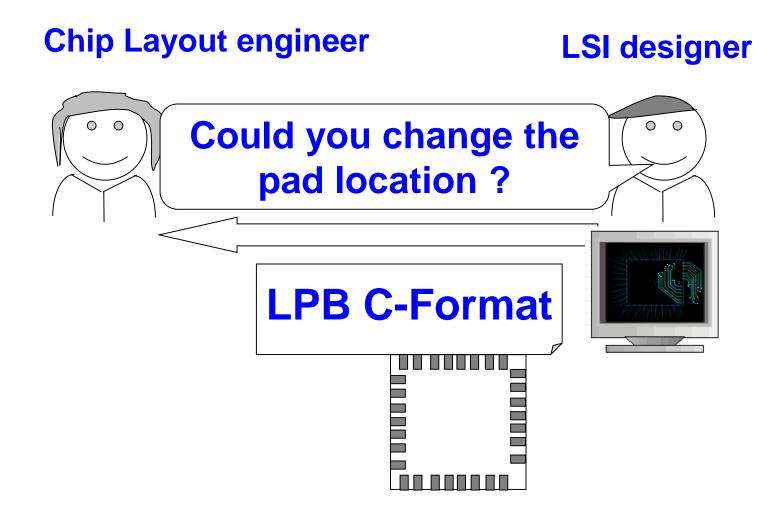
#### LSI designer



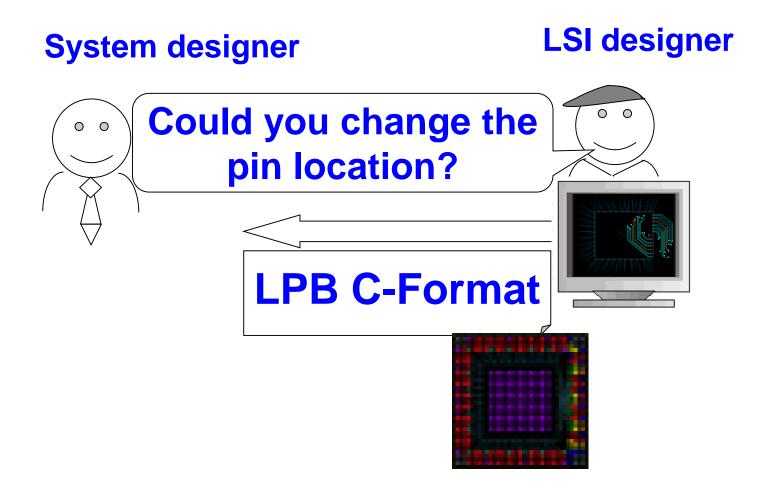
Read pin assignment from C-Format.



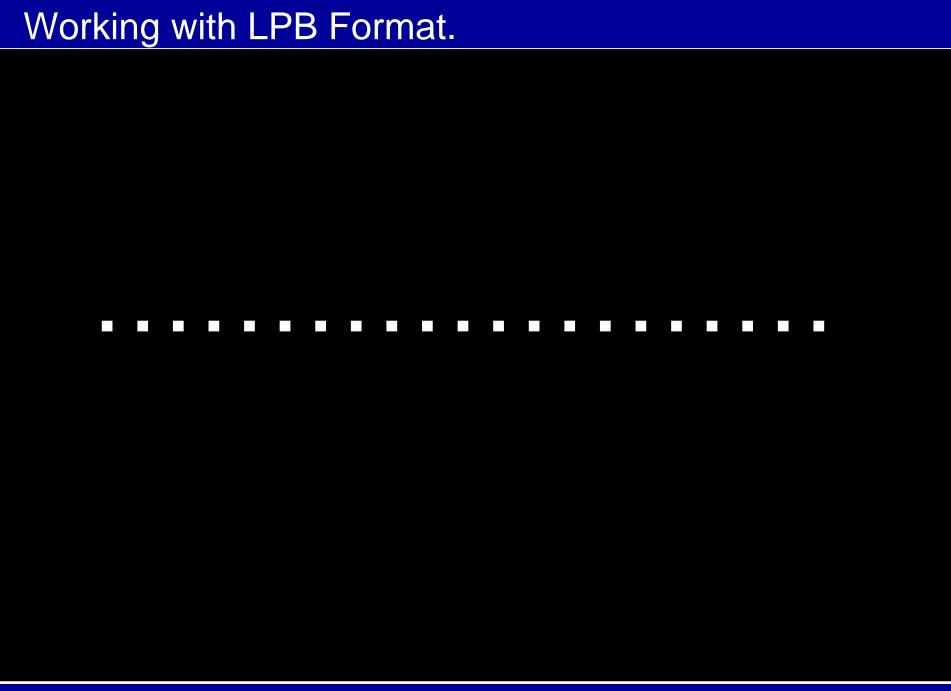
Consider trace routing in the package.



```
<shape>
</shape>
<padstack_def>
</padstack_def>
<module name="NEWLSI type="LSI"</pre>
shape_id="DieSize">
 <socket inst="IO">
   <default>
     <port_shape padstack_id="Pad" />
   </default>
   <port id="P11" name="DQ_0" x=".." y=".."/>
   <port id="P22" name="DQ_1" x=".." y=".."/>
 </socket>
</module>
```



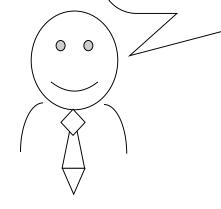
```
<module name="NEWLSI" type="PKG"</pre>
shape_id="BodySizeOfNEWLSI">
 <socket inst="IO">
   <default>
     <port_shape padstack_id="BallPad" />
   </default>
   <port name=DQ[0] id="D1" x=".." y=".."/>
   <port name=DQ[1] id="A2" x=".." y=".." />
 </socket>
</module>
```



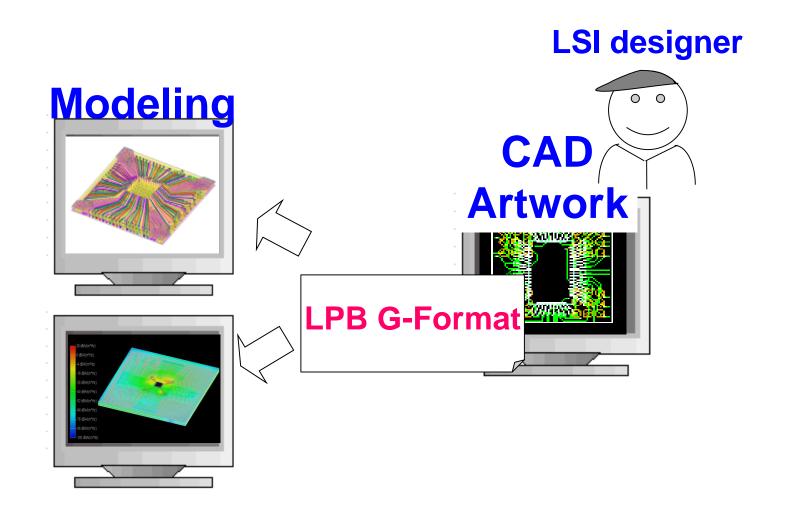
# System designer

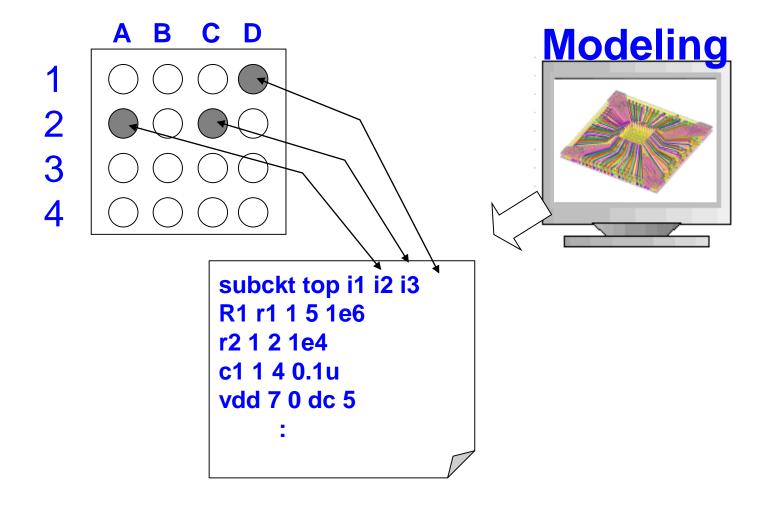
# LSI designer

Could you give me a package Model?



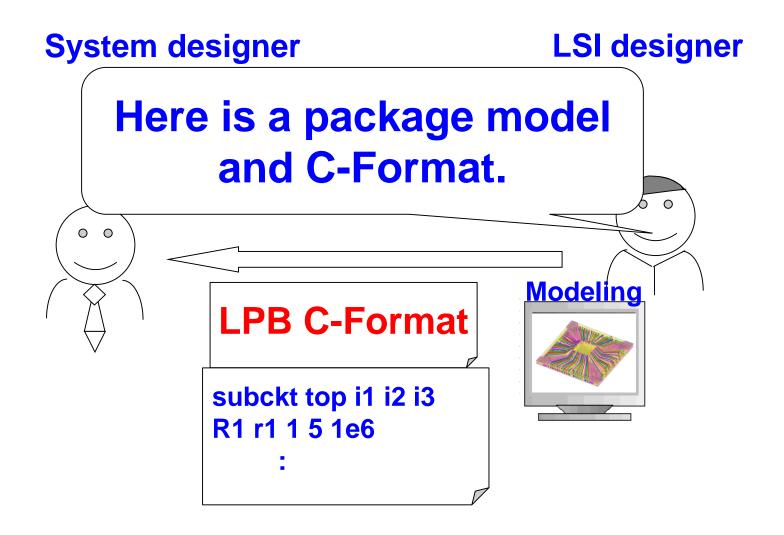






# Workin

```
Shape lu= bouysizeOhnevilsi >
<socket inst="IO">
   <default>
     <port_shape padstack_id="BallPad" />
   </default>
   <port name=DQ[0] id="D1" x=".." y=".."/>
   <port name=DQ[1] id="A2" x=".." y=".." />
</socket>
</module>
<reference reffile="NEWLSI.sp" format="SPICE">
<connect pirt_name="D1>
  <spice:ref_port subckt="top" portid="3"/>
</connect>
<connect pin_name="A2">
  <spice:ref_port subckt="top" portid="1"/>
 </connect>
</reference>
```



#### まとめ / 相互設計の課題とソリューション

- ■課題
  - ●相互設計 : 異文化同士の交流
    - コミュニケーションをもっとスムーズにしたい
  - ■異文化間交流には、定められたプロトコルが必要
    - 意思の疎通を円滑に・・・
  - 解析・モデリングツールを設計の道具に・・・
- ■ソリューション
  - ●コミュニケーションのためにフォーマットを統一 LPB M/N/C/G/R-Format

# 皆様のご協力を願います

# END