# Capacitive Values Extension for Std_logic_1164

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# Outline

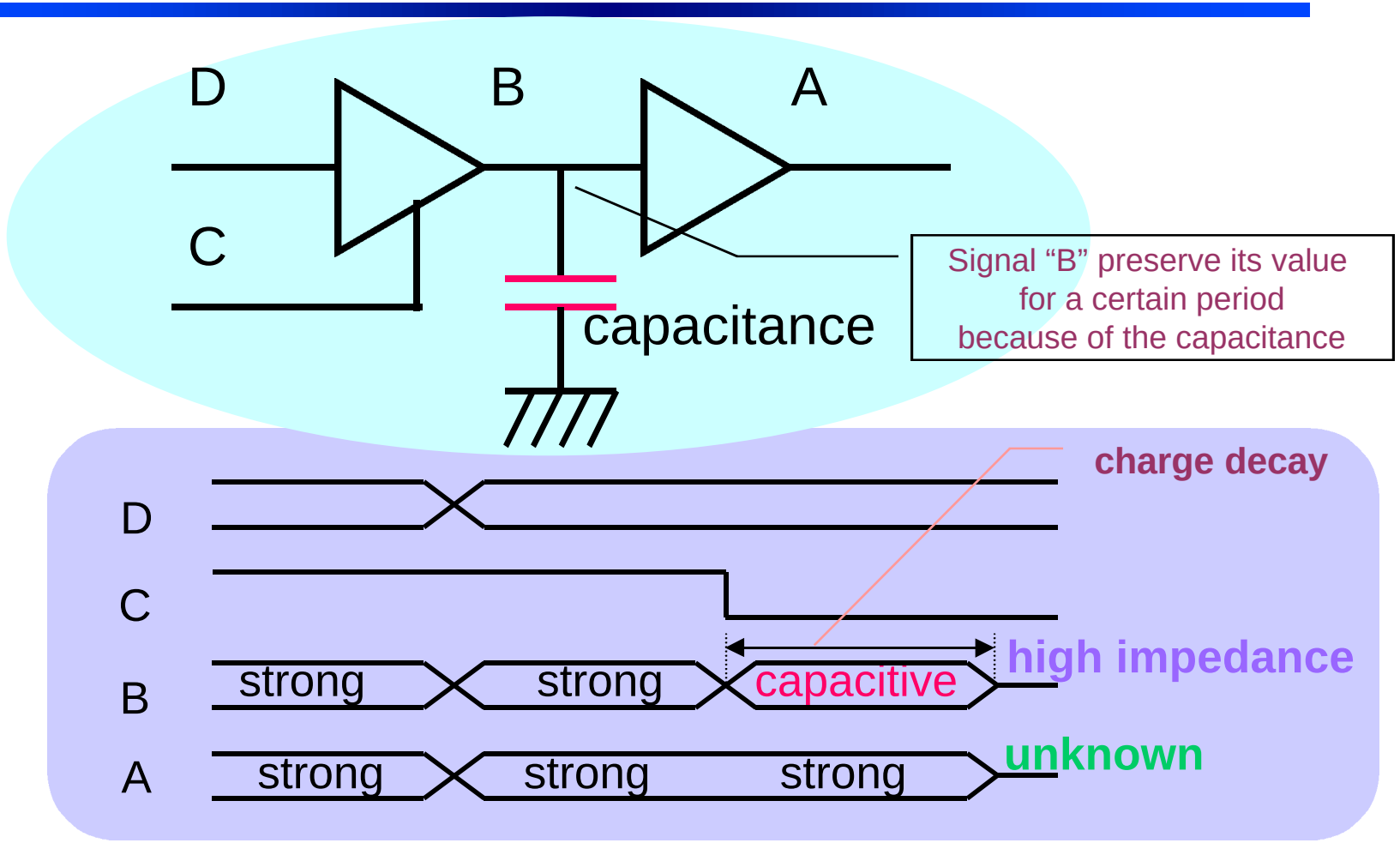
- 3 capacitive values
- Why capacitive values are required?
- Modification of package
- Dynamic behavior
- Impacts for current design environments
- Alternative extension
- Conclusion

# New Values in IEEE Std 1164

| Value / Strength | High | Low | Unknown |
|---|---|---|---|
| Initialize | U | | |
| Strong | 1 | 0 | X |
| Weak | H | L | W |
| **Capacitive** | **P** | **D** | **C** |
| High Impedance | Z | | |

```
TYPE std_ulogic IS
 ( 'U',   -- Uninitialized
   'X',   -- Forcing  Unknown
   '0',   -- Forcing  0
   '1',   -- Forcing  1
   'Z',   -- High Impedance
   'W',   -- Weak     Unknown
   'L',   -- Weak     0
   'H',   -- Weak     1
   '-',   -- Don't care
   'C',   -- Capacitive unknown
   'D',   -- Discharge 0
   'P'    -- Precharge 1
   );
```

# Why Capacitive Values Are Required?



# Why Capacitive Values Are Required?

- To model the dynamic circuits precisely, we have to consider the charge decay.
  - Delay time and power dissipation using MVL-9 are usually larger than those of real circuit.
  - Precise power calculation is requested to design mobile equipment.
  - Dynamic circuits are adopted in intellectual properties (IP).

# Candidates to Implement Capacitive Values

- IEEE Std 1164
  - (1) Declare new type.
  - (2) Modify "std_ulogic" type.
- IEEE Std 1076
  - (3) Change the specification of resolution function.
  - (4) Use special entity for capacitance.

# Modification of Std_logic_1164

- Preserve the name of package
- Add 3 capacitive values
- Re-declare tables, type-conversion functions & operations.

# Example of Resolution Table

```
CONSTANT resolution_table : stdlogic_table := (
--      ---------------------------------------------------------------------
--      |  U    X    0    1    Z    W    L    H    -    C    D    P         |   |
--      ---------------------------------------------------------------------
        ( 'U', 'U', 'U', 'U', 'U', 'U', 'U', 'U', 'U', 'U', 'U', 'U' ), -- | U |
        ( 'U', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X' ), -- | X |
        ( 'U', 'X', '0', 'X', '0', '0', '0', '0', 'X', '0', '0', '0' ), -- | 0 |
        ( 'U', 'X', 'X', '1', '1', '1', '1', '1', 'X', '1', '1', '1' ), -- | 1 |
        ( 'U', 'X', '0', '1', 'Z', 'W', 'L', 'H', 'X', 'C', 'D', 'P' ), -- | Z |
        ( 'U', 'X', '0', '1', 'W', 'W', 'W', 'W', 'X', 'W', 'W', 'W' ), -- | W |
        ( 'U', 'X', '0', '1', 'L', 'W', 'L', 'W', 'X', 'L', 'L', 'L' ), -- | L |
        ( 'U', 'X', '0', '1', 'H', 'W', 'W', 'H', 'X', 'H', 'H', 'H' ), -- | H |
        ( 'U', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X', 'X' ), -- | - |
        ( 'U', 'X', '0', '1', 'C', 'W', 'L', 'H', 'X', 'C', 'C', 'C' ), -- | C |
        ( 'U', 'X', '0', '1', 'D', 'W', 'L', 'H', 'X', 'C', 'D', 'C' ), -- | D |
        ( 'U', 'X', '0', '1', 'P', 'W', 'L', 'H', 'X', 'C', 'C', 'P' )  -- | P |
);
```

Original area

New values

Modified package is validated.

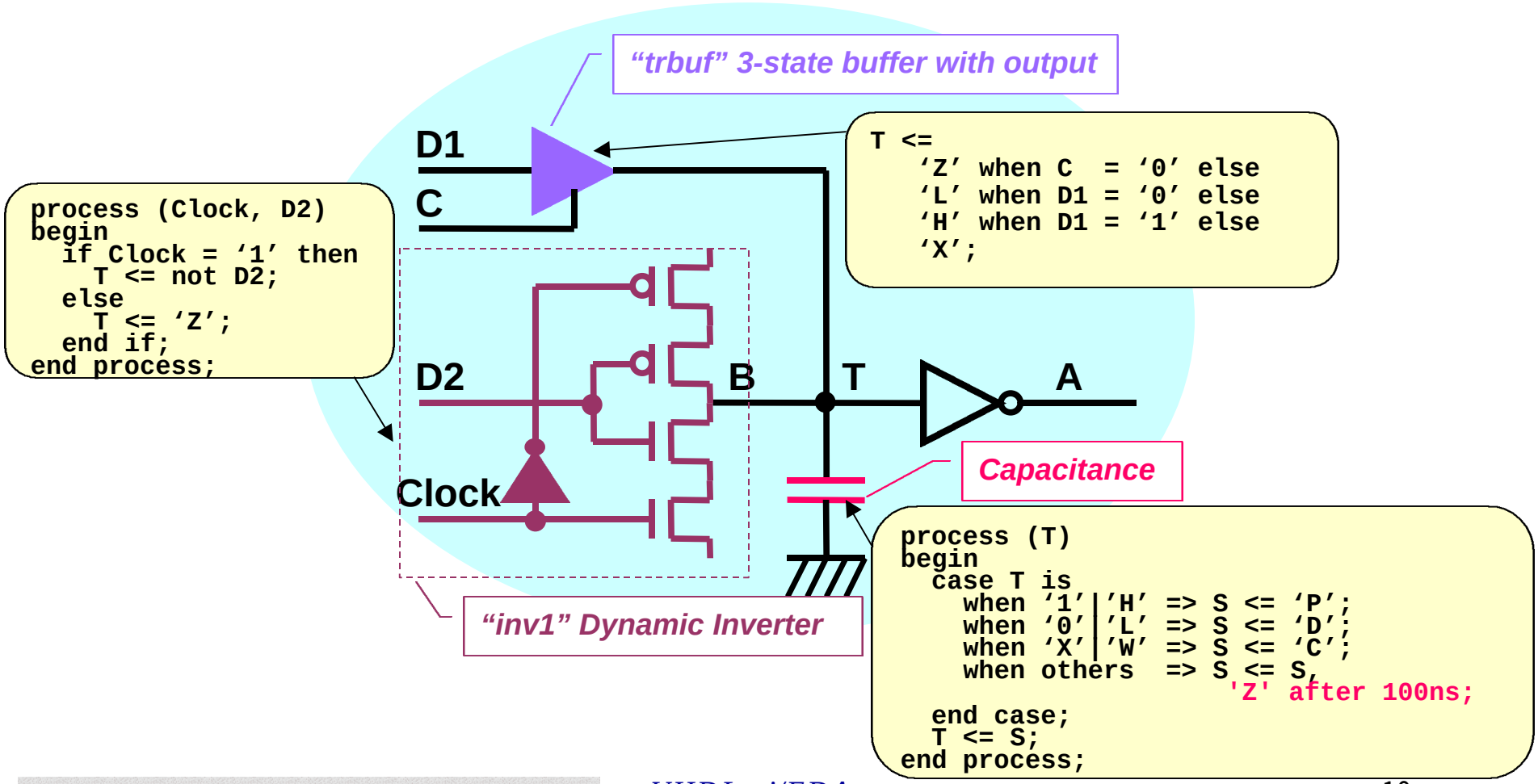
# Entity for Capacitance

- To model the dynamic circuits,we have to prepare the special entity, which has the behavior of capacitance.

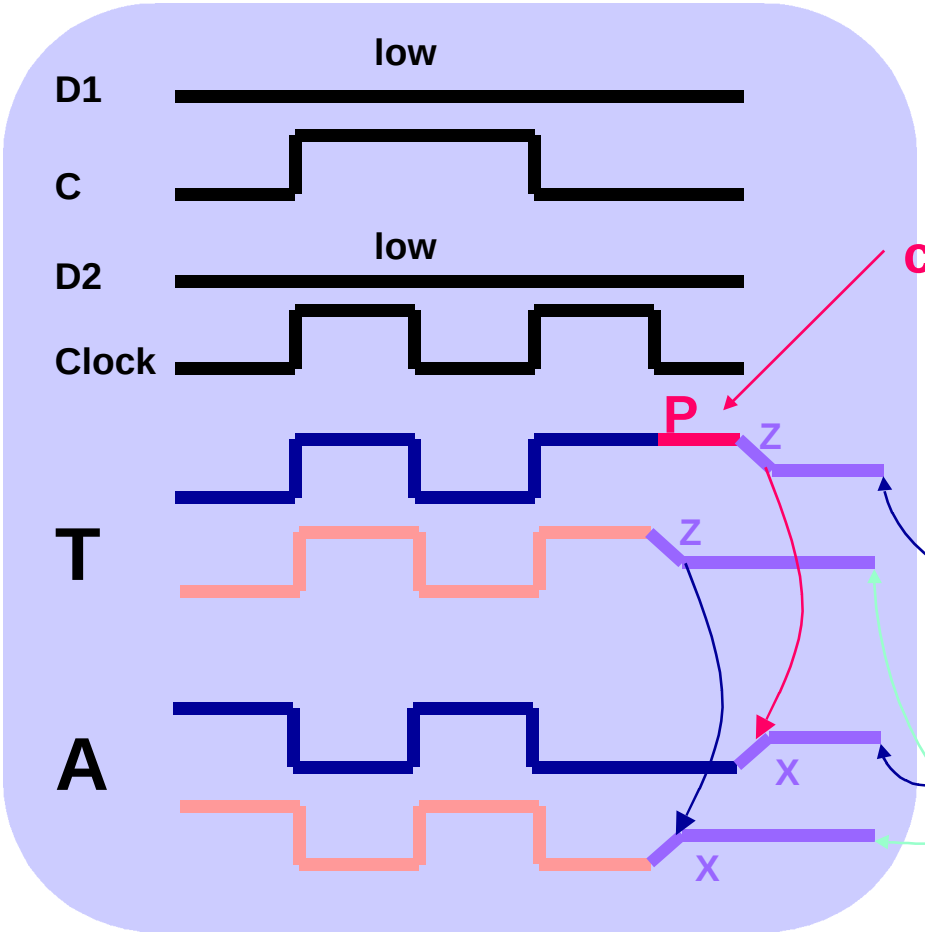
```
entity capacitance is
          generic (delay : time := 100ns);
        port (Tbus  : inout std_ulogic
        );
   end capacitance;

   architecture RTL of capacitance is
       signal Data : std_ulogic := 'Z';
   begin
       process(Tbus)
       begin
           case Tbus is
               when 'X'|'W' => Data <= 'C';
               when '0'|'L' => Data <= 'D';
               when '1'|'H' => Data <= 'P';
               when others  => Data <= Data, 'Z' after delay;
           end case;
           Tbus  <= Data;
       end process;
   end RTL;
```

# Example to Model Dynamic Circuit



# Expected Waveform




capacitive

**Expected waveform**
**MVL-12**

**Using current "std_ulogic"**
**MVL-9**

# Impacts for Design Environments

- VHDL language (IEEE Std 1076)
  - None
- Standard library (IEEE Std 1164)
  - Change name of type, type-conversion functions and operations.
- VITAL (IEEE Std 1076.4) & SDF
  - The considerable discussions should be done, but not finished yet.
- EDA tools
  - Tools should be optimized for the new package.

# Alternative Extension

- Change the specification of resolution function

```
impure function charged(driver: in std_ulogic_vector) return std_ulogic is
        alias previous: std_ulogic is charged'resolved_signal;
        signal resolved: std_ulogic;
        variable tmp: std_ulogic:= 'Z';
    begin
        -- resolve all inputs by static analysis (first stage)
        for i in driver'range loop
            tmp := resolution_table(tmp, driver(i));
        end loop;
        -- consider charge decay behavior when Hi-Z (second stage)
        if tmp = 'Z' then
            case previous is
              when 'X'|'W' => resolved <= 'C', 'Z' after previous'decay_time;
              when '0'|'L' => resolved <= 'D', 'Z' after previous'decay_time;
              when '1'|'H' => resolved <= 'P', 'Z' after previous'decay_time;
              when others  => resolved <= 'Z';
            end case;
        else
            resolved <= tmp;
        end if;
        return(resolved);
    end;
```

# Conclusion

- We proposed that 3 capacitive values should be added into the standard values in IEEE Std 1164.
- The behavior of the realistic circuits is illustrated, and validated in VHDL-pj/EIAJ.
  - The modified package and test descriptions are available. Please contact to authors. (Email:kaba@lsi.nec.co.jp)
- This extension will be essential for the model of dynamic circuits precisely.